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## **Post-Processed Integrated Microsystems**

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### **Abstract**

This report represents the completion of a three-year Laboratory-Directed Research and Development (LDRD) program to develop a low cost platform for integrated microsystems that is easily configured to meet a wide variety of specific applications-driven needs. Once developed, this platform, which incorporates many of the elements that are common to numerous microsystems, will enable integrated microsystem users access to this technology without paying the high up-front development costs that are now required. The process starts with the fabrication, or acquisition, of wafers which have sparsely placed device or circuit components fabricated in any foundried technology (Si CMOS or bipolar technologies, high-frequency GaAs technologies, MEMS, etc.). We call these “smart substrates.” Using the diverse processing capabilities of SNL, we then intend to “post-process” high-value components in open areas on the front or back of the wafers and microelectronically integrate the added components with the pre-placed circuitry. Examples of post-processed components include sensors, antennas, SAW devices, passive elements, micro-optics, and surface-mounted hybrids. The combination of pre-placed electronics and post-processed components will enable the development of many new types of integrated microsystems. Targeted applications include integrated sensor systems, tags, and electromechanical systems.

**Keywords:** microelectromechanical systems (MEMS), micro-optoelectromechanical systems (MOEMS), integrated microsystems, sensors, flexural plate wave (FPW), microsystem, deep reactive ion etching (DRIE), advanced packaging, surface acoustic wave (SAW), chemiresistor

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## INTRODUCTION

Advanced optoelectromechanical system design is constantly pushing for higher levels of functionality and reliability with lower system size, weight, power, and cost. To achieve these goals, many system designs are envisioned as fully integrated “microsystems-on-a-chip”. This level of integration is often hard to realize because of the necessity of combining different devices made with diverse materials and processes, all in a single microelectronic technology (i.e., silicon CMOS).

Here we propose a simpler, faster, and more cost-effective approach to integrated microsystem design that addresses many of these problems. The process starts with the fabrication, or acquisition, of wafers with sparsely placed device or circuit components fabricated in any foundried technology (Si CMOS or bipolar technologies, high-frequency GaAs technologies, MEMS, etc.). We call these “smart substrates”. Using the diverse processing capabilities of SNL, we then intend to “post-process” (i.e., to interrupt a microelectronic production sequence in mid stream and do something unique) high-value components in open areas on the front or back of the wafers and microelectronically integrate the added components with the pre-placed circuitry. Examples of post-processed components include sensors, antennas, SAW devices, LIGA-formed components, passive elements, micro-optics, and surface-mounted hybrids. The combination of pre-placed electronics and post-processed components will enable the development of many new types of integrated microsystems. Targeted applications include integrated sensors and control electronics, electromechanical systems, and tags.

This is a new approach to integrated microsystem development which exploits SNL’s extensive foundry-like capabilities for fabricating Si or GaAs integrated circuits as well as our ability to do pre- or post-processing. It is a way of leveraging all of the processing resources of SNL to fabricate applications-specific integrated microsystems.

The economy and flexibility of this approach comes from different areas. For many systems, the smart substrates can be generic platforms upon which many different types of integrated systems can be constructed. Small-lot economy and simplicity also arise from the concept of “mixed processing”. (Letting each laboratory (the MDL and CSRL, for example), concentrate on the processes and production sequences they are most familiar with.) Economy and flexibility can also be achieved by reducing design/fabrication cycle time. This can often be achieved by isolating and post-processing the speculative or sensitive components in the system. With proper design of the smart substrate, the speculative components can be redesigned and post-fabricated faster than the time it would take to redesign and fabricate one iteration of a fully custom system.

An excellent example of this design approach is the integrated sensed microsystem shown in Figure 1). The drawing shows a Si CMOS integrated circuit that contains generic systems-specific control electronics and switching circuitry. Two thirds of the wafer surface will be left unpopulated with electronics. A wafer lot of circuits will then be fabricated and removed from the normal CMOS production sequence just prior to dicing and packaging. Wafers will then be taken to the CSRL where arrays of flexural plate wave (FPW) sensors will be microelectronically formed, completing the fabrication cycle. FPW devices are very suitable for this application because of (a) high mass sensitivity at low operating frequencies (simplifying electronics), (b) materials compatibility with Si IC processing, (c) separation of sensor and electronics from analyte stream, (d) possibility of liquid operation (important for many bio-sensor applications), and (e) the possibility of pumping (or sample handling). If test and

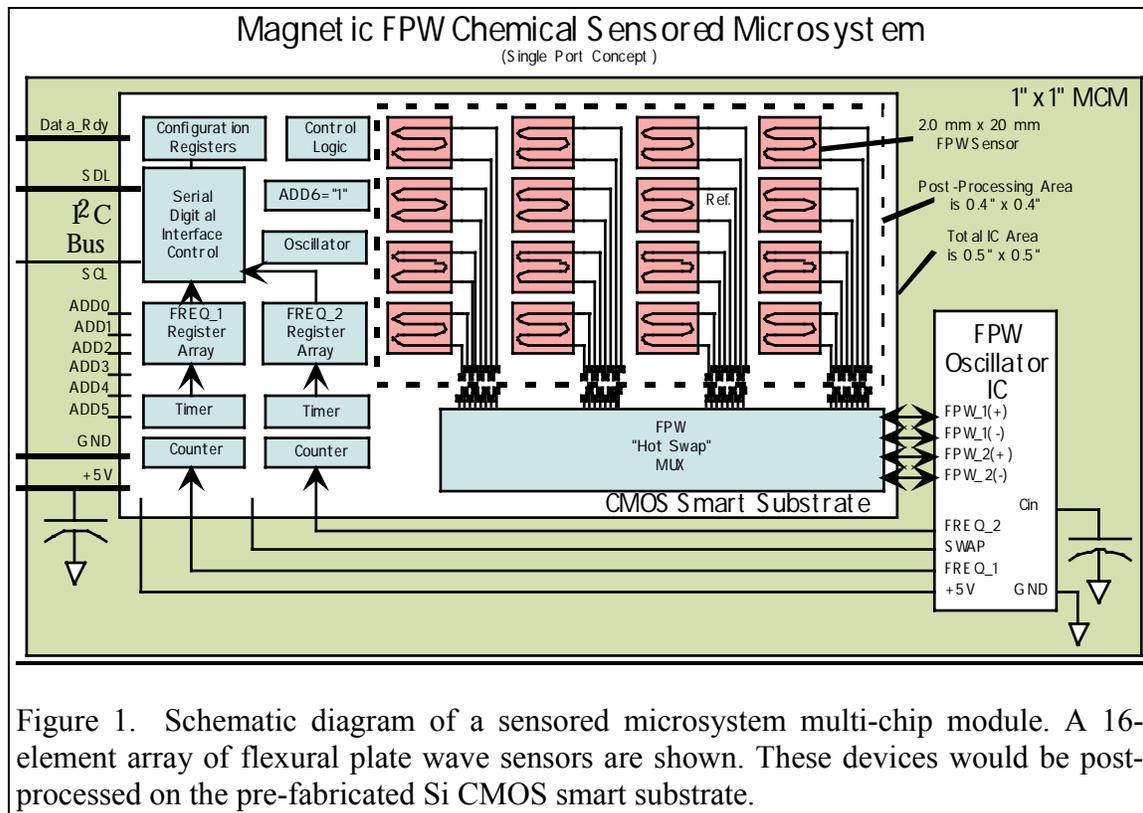


Figure 1. Schematic diagram of a sensored microsystem multi-chip module. A 16-element array of flexural plate wave sensors are shown. These devices would be post-processed on the pre-fabricated Si CMOS smart substrate.

evaluation shows that the FPW devices need redesign, the post processes and artwork will be redone, and the system fabrication cycle will be restarted on additional smart substrates from the production lot.

This design approach is conceptually amenable to a large number of integrated microsystems being designed to meet DOE, DOD, and National Security needs. A second example of a post-processed integrated microsystem is the surety component shown in Figure 2). Using high-aspect-ratio etched silicon a self-assembled and self-packaged LIGA micromachine can be fabricated. The silicon wafer can be micromachined to accommodate two layers of drop-in LIGA microstructures, along with coils and an optical monitor. The two LIGA microstructures can be made separately; using LIGA x-ray lithography techniques, brought whole to the silicon wafer, and dropped into place. These LIGA structures can then be released, forming a complete self-assembled microdiscriminator. A second wafer, with preplaced drive electronics, can be micromachined on the front side to provide a mating surface for the opposing wafer. These two wafers can then be brought together and bonded to form an inexpensive silicon package, containing a complete integrated microsystem.

This project recognizes and brings together a diverse collection of microelectronic technology development activities that are occurring all across Sandia. It recognizes, and exploits the fact that we have significant prototyping resources for both Si- and GaAs-based ICs. It further exploits the concept that we have highly flexible fabrication resources that can continue microelectronic processing sequences "after the fact". There are constraints on both smart substrate fabrication and post-processes that must be mentioned, however. First, the processing yield on any circuitry considered for a smart substrate must be very high. "Functionality" at this point must be a given, as there will be serious yield limiting steps

associated with the post-fabrication of other speculative components. Second, the post-processes themselves must not damage the pre-placed circuitry. Understanding process interferences between the smart substrates and post-processed components will be a major challenge.

A potpourri of acceptable post-processes has already been identified. These include thin film metallization and dielectric deposition technologies, various via etch processes for both Si and GaAs, deep trench etching technologies for a variety of substrate materials, flip chip bonding of foreign components, heat pipe technologies, etc. An intriguing possibility involves the inclusion of LIGA-formed micromechanical components as a post-processing option. Combining all of these processes can enable the two microsystem “visions” shown in Figures 1) & 2).

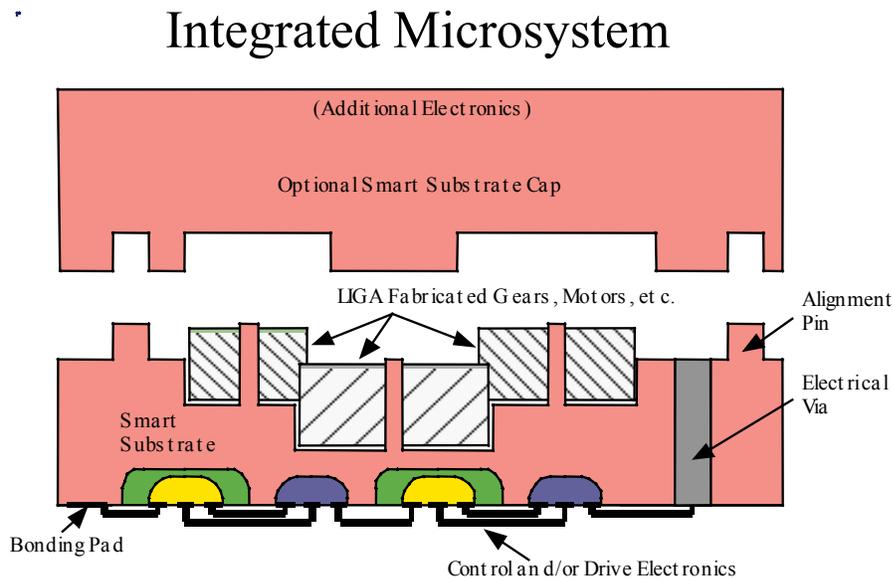


Figure 2. Stylized schematic representation of an integrated microsystem formed from post-processed, LIGA-fabricated, micromechanical components.

**PROCESS DEVELOPMENT AND INTEGRATION:**

Key process capabilities have been identified, optimized and applied to establish a post-processing capability in the CSRL. Metal plating and electron-beam evaporation processes have been identified and developed for both thick (> 1µm) and thin film applications of post-processed wafers. For example, MEMS structures fabricated in the MDL have been plated with evaporated Au to enable light-steering devices. Additionally, evaporated seed metals and plated metals are currently being evaluated for through wafer electrical interconnects (Ni and Au). Low stress (< 100 MPa) Si<sub>3</sub>N<sub>4</sub> and composite SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub> PECVD films are being developed for insulating films in through wafer vias and as membranes in flexural plate wave (FPW) devices (sensors, actuators, heaters, etc.). In addition thermal (steam) oxide films have been developed in the CSRL and have shown promising results for insulator and membrane structures.

*Metallization*

Post-processed metallization of MEMS structures has been demonstrated in the CSRL using two techniques; lithographic metallization and shadow masking. The advantages of

lithographic metallization are fine alignment tolerances, relatively small feature size, and further processing of the device. However, additional processing steps complicate the process and it must be compatible with the MEMS release process. The lithographic metallization process is shown schematically in Figure 3. Windows are defined in the  $\text{SiO}_2$  film lithographically resulting in tight alignment tolerances. The oxide is then etched using either a wet chemical or a dry etch process down to the polysilicon layer. A lift-off metallization process is then used to pattern the exposed poly-Si with Au. This process is pre-release so the MEMS structures are encapsulated and protected throughout the metallization steps

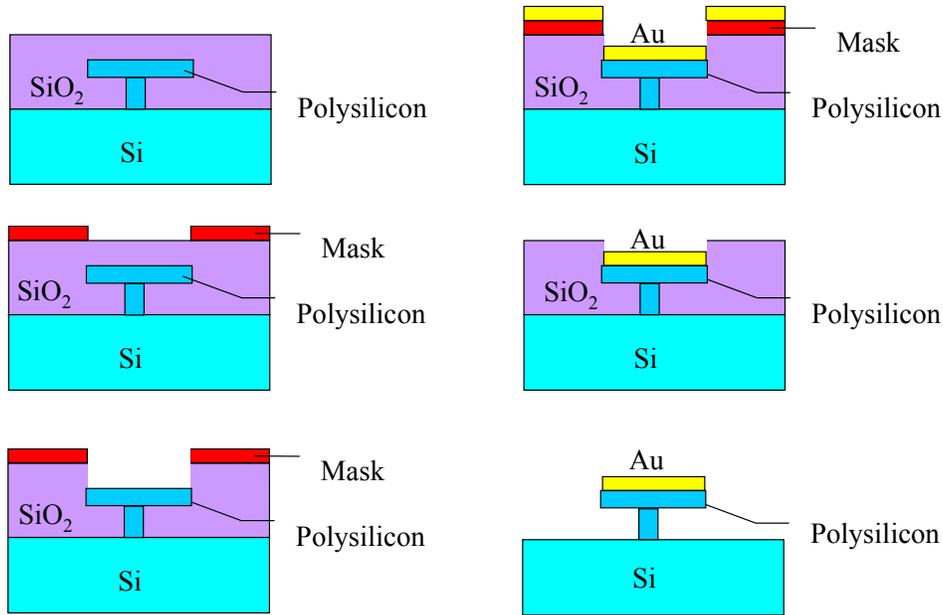


Figure 3. Schematic diagram of metallization using lithography. The metal is deposited prior to release of the MEMS devices leading to further process steps.

By contrast, the shadow mask metallization process is simpler and more established. However, this process yields crude alignment tolerances, requires large feature sizes and because the shadow mask process is done following release of the MEMS structures, great care is necessary in handling the device and further processing is not possible. The shadow mask process is shown schematically in Figure 4. The MEMS sample is mounted into a fixture with alignment tolerances of several microns. The shadow mask, which can be made of several materials including Si, is then aligned relative to the MEMS feature and physically attached to the fixture. The assembly is then placed in an evaporator for metal deposition. Since the deposition is line of sight only the open areas of the MEMS sample defined by the shadow mask are metallized.

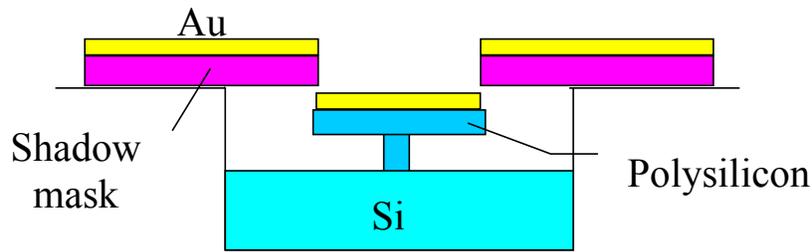


Figure 4. Schematic diagram of shadow mask metallization scheme. The metallization is deposited following release of the MEMS device.

#### *Deep Reactive Ion Etching (DRIE)*

The ability to etch deep, high-aspect ratio, anisotropic Si features has revolutionized the conception and implementation of “mixed technology” integration and packaging. The development of integrated microsystems and advanced packaging capabilities in an integrated circuit (IC) batch manufacturing technology will lower cost, reduce size and weight, and improve performance and reliability.<sup>1</sup> A complete integrated microsystem could include sensors, actuators, electronics, fluidics, and optics in a variety of material systems on a single chip or in a single package. For example, deep anisotropic features could be etched into a Si wafer to accurately locate discrete components while maintaining system planarity.

The fabrication and integration of MEMS, both mechanical and fluidic structures, with electronic and photonic devices relies heavily on two patterning techniques, surface micromachining and bulk silicon micromachining. A comparison of the two techniques is given by French and Sarro.<sup>2</sup> In many ways the deep silicon trench-etching technology discussed here enables the integration of the best aspects of each of these technologies.

Bulk silicon micromachining refers to the etching of deep, Si features that can be up to and including the thickness of the wafer. Initial work in this area was performed using wet etches for either isotropic or anisotropic profiles. Isotropic etching was often achieved with mixtures of nitric, hydrofluoric and acetic acids while anisotropic profiles were obtained using hydroxide based mixtures. Anisotropic wet etches are highly dependent upon crystallographic orientation. While very impressive structures can be fabricated using this type of process, the technique is limited by the crystallography of the material. It is possible to etch through-holes using this technique and the creation of relatively massive structures is possible. However, there are limitations on the geometry’s feasibility and high fidelity is typically not possible.

Recently, new bulk Si micromachining processes based on a high etch rate has been developed. This approach addresses many of the limitations of wet chemical micromachining since the pattern fidelity is not limited by crystallography, selectivity, or directionality. To date, most work reported in the literature in this area has been done with research tools, or with very large features.<sup>3, 4</sup> The utilization of high-density plasmas (HDP) including electron cyclotron resonance (ECR) and inductively coupled plasma (ICP) etch systems and the development of the “Bosch” deep reactive ion etch (DRIE) process<sup>5</sup> has contributed significantly to the development of high-aspect ratio, deep Si etching.<sup>6-11</sup> HDP etch systems typically yield higher etch rates under less energetic ion conditions than more conventional reactive ion etch (RIE) systems. This has been attributed to plasma densities that are 2 to 4 orders of magnitude higher and the ability to effectively decouple ion energy and plasma density. Etch profiles also tend to be more

anisotropic due to lower process pressures which results in less collisional scattering and greater directionality of the plasma species.

As mentioned above, pattern transfer into Si has been very successful by both wet chemical and plasma etch techniques. However, the fabrication of deep, high-aspect ratio Si structures has been limited due to low etch selectivity to photoresist masks, slow etch rates, or poor lateral dimensional control. The recent development of the DRIE Si etch process has resulted in anisotropic profiles at room temperature, etch rates  $> 3.0 \mu\text{m}/\text{min}$ , aspect ratios  $> 30:1$ , and good dimensional control.<sup>5-11</sup> Additionally, the DRIE process has shown etch selectivities of Si to photoresist  $\sim 100:1$  thereby eliminating the process complexity of hard etch masks for features deeper than  $100 \mu\text{m}$ .

The DRIE process (patented by Robert Bosch GmbH)<sup>5</sup> relies on an iterative ICP-based deposition/etch cycle in which a polymer etch inhibitor is conformally deposited over the wafer during the deposition cycle. This is displayed schematically in Figure 5. The polymer deposits over the resist mask, the exposed Si field, and along the sidewall. During the ensuing etch cycle, the polymer film is preferentially sputtered from the Si trenches and the top of the resist mask due to the acceleration of ions (formed in the ICP plasma) perpendicular to the surface of the wafer. Provided the ion scattering is relatively low, the polymer film on the sidewall is removed at a much slower rate, thus minimizing lateral etching of the Si. Before the sidewall polymer is completely removed, the deposition step is repeated and the cycle continues until the desired etch depth is obtained.

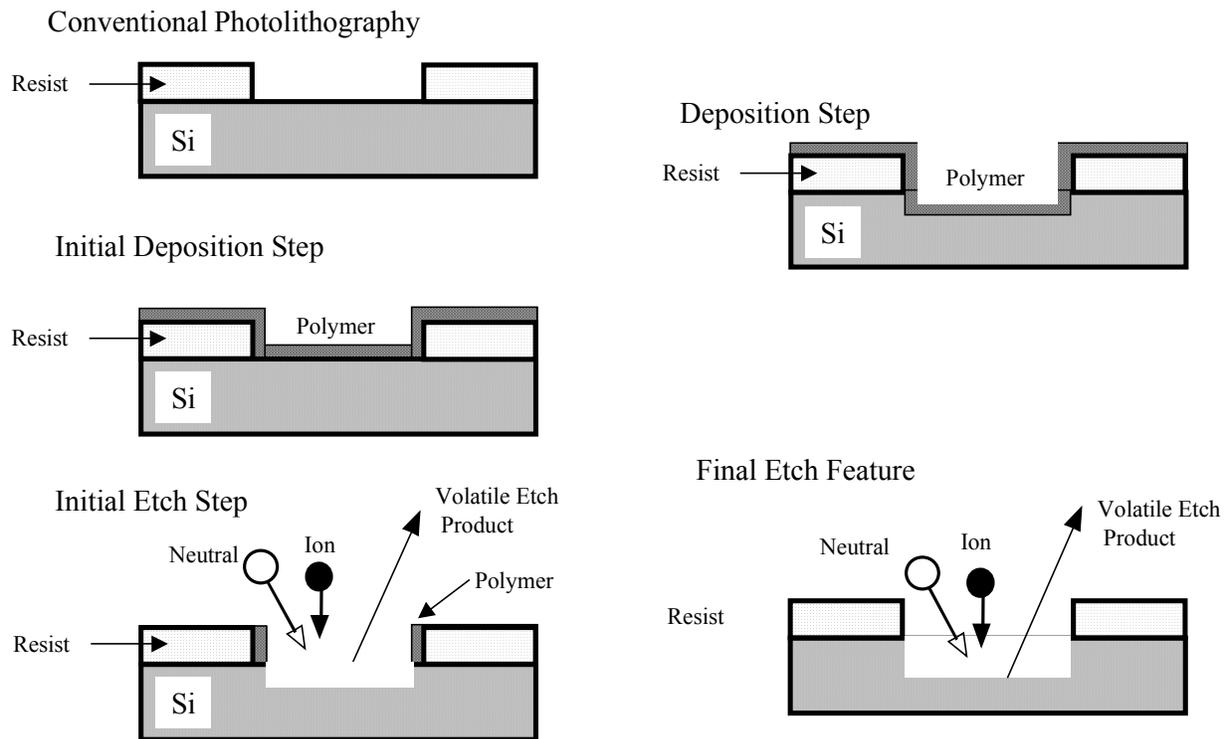


Figure 5. Schematic diagram of the deep reactive ion etch (DRIE) “Bosch” process.

### *DRIE versus ICP etch comparison*

In Figure 6, SEM micrographs show Si vias etched by (a) the DRIE process and (b) an ICP-generated SF<sub>6</sub>/O<sub>2</sub> plasma. The via etched using the DRIE process was approximately 40 μm wide and etched to a depth of approximately 70 μm while the vias etched in the ICP were 50 μm wide and etched to a depth of approximately 150 μm. The DRIE etch conditions were 23 mTorr pressure, 100 sccm SF<sub>6</sub>, 40 sccm Ar, 875 W ICP source power, 6 W cathode rf-power with a corresponding dc-bias of -25 to -50 V, and 20°C substrate temperature. The DRIE deposition conditions were 22 mTorr pressure, 70 sccm C<sub>4</sub>F<sub>8</sub>, 40 sccm Ar, 875 W ICP source power, 1 W cathode rf-power with a corresponding dc-bias of approximately -5 V, and 20°C substrate temperature. The ICP etch conditions were 5 mTorr pressure, 50 sccm SF<sub>6</sub>, 10 sccm O<sub>2</sub>, 10 sccm Ar, 500 W ICP source power, 250 W cathode rf-power with a corresponding dc-bias of -350 V, and -40°C substrate temperature. Due to the high dc-bias used in the ICP, the etch selectivity of Si to photoresist was typically < 2:1; therefore, a Ni mask was used to achieve etch depths > 25 μm. The Si etch rate obtained in the ICP was approximately 1 μm/min. The DRIE process used a photoresist mask due to etch selectivities of Si to photoresist > 75:1. The high etch selectivity was attributed to the deposition of the sidewall polymer etch inhibitor, which also deposited on the resist. Despite ion bombardment of the surface, the deposited polymer significantly reduced the erosion rate of the resist thereby improving the etch selectivity. Additionally, the DRIE process required much lower dc-biases than the ICP (< -50 V as compared to -350 V) that significantly reduced the resist erosion rate. The DRIE process yielded an etch rate of approximately 2.0 μm/min with highly anisotropic etch profiles, good dimensional control, and smooth etch morphologies. The sidewall polymer etch inhibitor deposited in the DRIE process eliminated lateral etching of the Si resulting in via widths which were essentially identical at the top and bottom of the feature and maintained the dimensions of the resist pattern. However in the ICP, lateral etching of the Si was observed due to the absence of a sidewall polymer; this

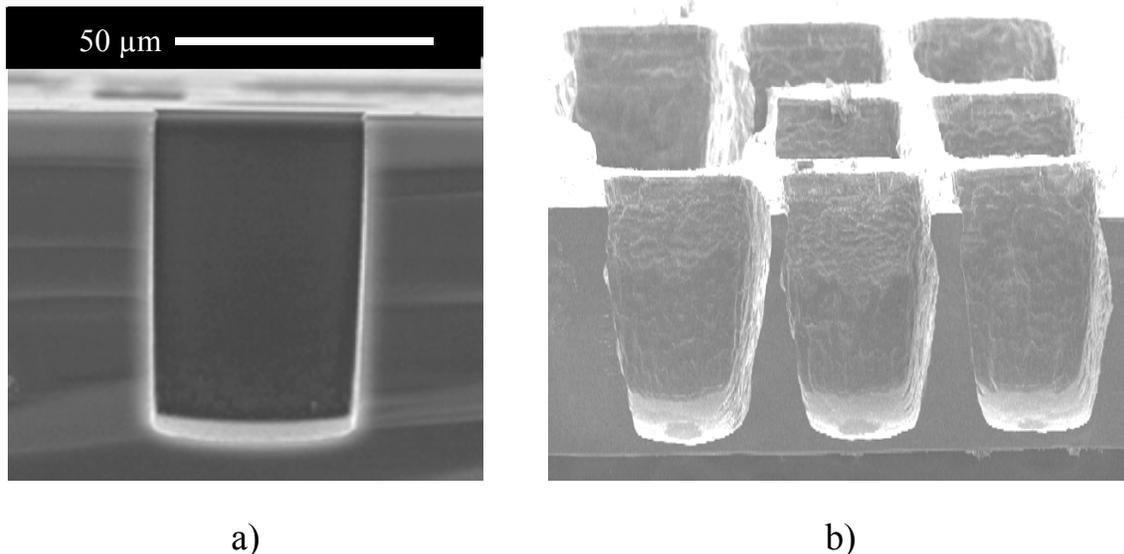


Figure 6. SEM micrographs which show Si vias etched by (a) the DRIE process and (b) an ICP-generated SF<sub>6</sub>/O<sub>2</sub> plasma. The via etched using the DRIE process was approximately 40 μm wide and etched to a depth of approximately 70 μm while the vias etched in the ICP were 50 μm wide and etched to a depth of approximately 150 μm.

resulted in a concave sidewall profile with a much wider opening at the top of the via than that obtained at the bottom. Additionally, the sidewall was much rougher than that achieved using the DRIE process. The lateral Si etching observed in the ICP was somewhat surprising due to the low process pressure (2 mTorr), which reduces ion scattering and sidewall sputtering, and the low substrate temperature (-40°C) which lowers the volatility of the etch products.

#### *Etch rates and selectivity to masking materials*

Si etch rates and selectivity to resist were evaluated for the DRIE process as a function of chamber pressure, cathode rf-power, ICP source power, and SF<sub>6</sub> flow rate. In Figure 7, Si etch rates and etch selectivity of Si to photoresist are shown as a function of pressure while the cathode rf-power, ICP source power, gas flows, substrate temperature, and deposition parameters remained constant. Plasma conditions change quite dramatically as a function of pressure. In particular, with increasing pressure the mean free path decreases, the collisional frequency increases, and the residence time of the reactive species increases. This typically results in changes in both ion energy and plasma density which strongly influence the etch properties. In the DRIE process, Si etch rates increased as the pressure was increased from 15 to 20 mTorr, suggesting a reactant-limited regime at low pressures. Above 20 mTorr, the Si etch rate was relatively independent of pressure. Selectivity of Si to photoresist was typically > 50:1 with a maximum of approximately 95:1 at 25 mTorr. Etch profile and morphology were typically anisotropic and smooth and relatively independent of pressure.

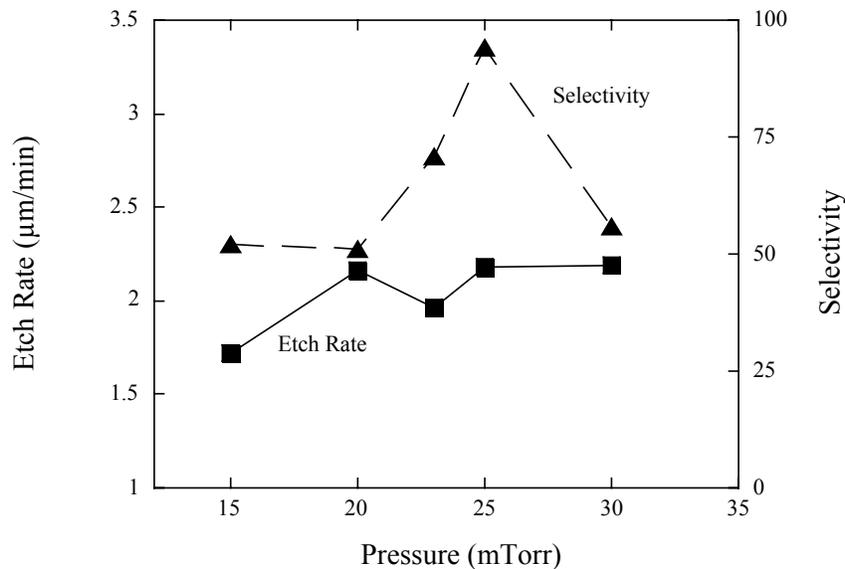


Figure 7. Si etch rates and etch selectivity of Si to photoresist as a function of pressure in the DRIE process.

In Figure 8, Si etch rates and etch selectivity of Si to photoresist are plotted as a function of cathode rf-power for the DRIE process. All other etch and deposition parameters remained constant. Si etch rates increased by almost a factor of 3 as the cathode rf-power increased. Cathode rf-power is closely related to dc-bias and ion bombardment energy. Faster etch rates at

higher dc-bias implies more efficient bond breaking of the Si surface bonds and improved sputter desorption of the etch products (i.e.  $\text{SiF}_x$ ) from the surface. Additionally, as the ion bombardment energy increased so did the sputtering efficiency of the polymer in the Si field, which was deposited during the deposition cycle of the DRIE process. Under low rf-power conditions, the polymer may not sputter as efficiently thereby reducing the Si etch rates. Despite faster Si etch rates, the etch selectivity decreased quite dramatically as the cathode rf-power increased due to faster sputter rates of the polymer and faster erosion rates of the resist.

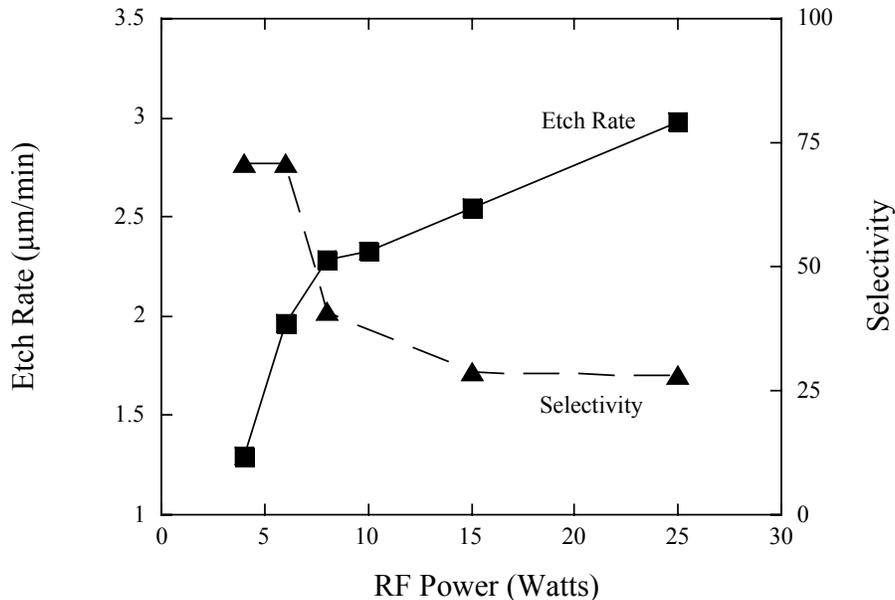


Figure 8. Si etch rates and etch selectivity of Si to photoresist as a function of cathode rf-power for the DRIE process.

Dimensional control and etch profile can also be strongly dependent on cathode rf-power. Under low cathode rf-power conditions, the etch profile was positively tapered. At moderate cathode rf-powers, the profile was highly anisotropic. Finally, under high cathode rf-power conditions, the profile became re-entrant. This trend can be observed in Figures 9 and 10. In Figure 9, SEM micrographs show Si posts etched at (a) 8 and (b) 25 W cathode rf-power. At 8 W, the etch profile was highly anisotropic at an etch depth of approximately  $23\ \mu\text{m}$ . At 25 W, the etch depth was approximately  $30\ \mu\text{m}$  and a prominent re-entrant profile was observed. The re-entrant profile observed under high rf-power conditions was attributed to more ion scattering at the base of the feature and higher sputter removal rates of the polymer from the Si sidewall.

In Figure 10, Si trenches  $15$  to  $20\ \mu\text{m}$  wide were etched approximately  $70\ \mu\text{m}$  deep. In Figure 10a, the DRIE process was operated at 6 W cathode rf-power for 30 minutes. The etch rate was approximately  $2\ \mu\text{m}/\text{min}$  at a dc-bias of approximately  $-50\ \text{V}$ . The trench profile was positively tapered with significant roughness at the bottom; however, the sidewall at the top of the trench remained smooth while maintaining the critical dimensions. The rough etch morphology at the bottom of the trench was attributed to inefficient sputter removal of the deposited polymer due to ineffective ion transport. In Figure 10b the DRIE process was separated into 3 steps, 1) the standard process (6W cathode rf-power) for 20 minutes followed by 2) a 5 minute etch step at 8W cathode rf-power and 22% longer etch time and then 3) the

standard process for 5 minutes. The etch was approximately 15  $\mu\text{m}$  deeper than the single step etch process with an etch rate of approximately 2.5  $\mu\text{m}/\text{min}$ . The etch was highly anisotropic

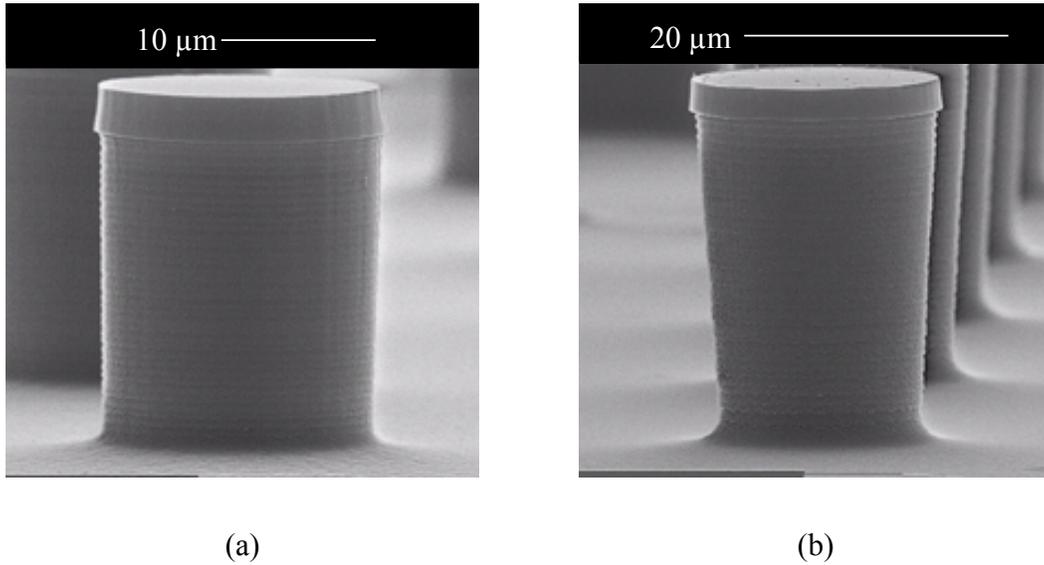


Figure 9. SEM micrograph of Si posts DRIE etched at (a) 8 W and (b) 25 W cathode rf-power. The re-entrant profile observed at 25 W cathode rf-power was attributed to increased ion scattering and sputter removal of the sidewall polymer.

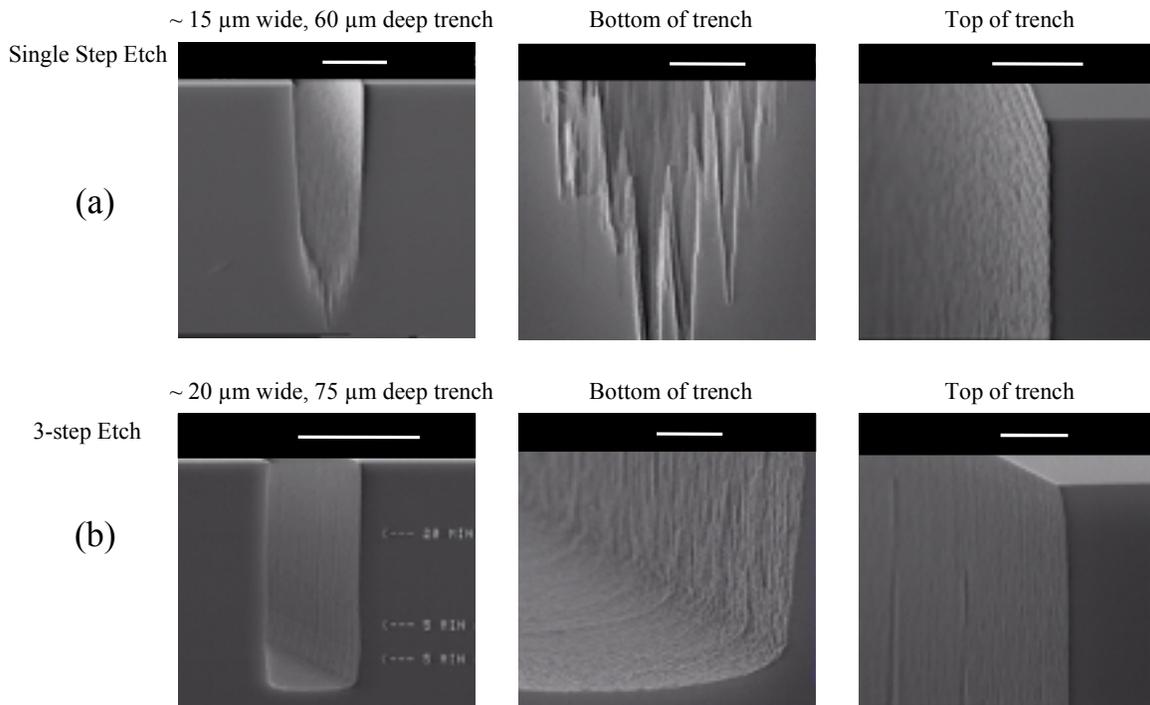


Figure 10. SEM micrograph of Si etched with a) single step DRIE process (6W cathode rf-power) and b) a three-step DRIE process with an aggressive step (8W cathode rf-power) to increase the sputter desorption at the base of the trench.

with a slight foot at the base of the sidewall and a smooth sidewall morphology throughout the feature. At higher rf-power, the increased ion bombardment energy improved the sputter removal of the deposited polymer from the bottom of the trench and allowed chemical etching at the base of the Si trench. Therefore feature size and density plays a critical role in the DRIE etch results. As observed in Figure 10, the etch/deposition cycles must be carefully balanced in the DRIE process.

Etch results can also have a strong dependence on ICP source power due to 1) the change in concentration of reactive species which influences the chemical component of the etch mechanism and 2) changes in ion flux which influences the physical sputter component of the etch mechanism. Si etch rates increased by approximately 30% as the ICP source power increased. The Si etch selectivity to photoresist ranged from approximately 55:1 to 90:1 for ICP powers from 750 to 950 W. Etch profiles were slightly re-entrant and rough under low ICP source power conditions, but highly anisotropic and smooth under moderate to high ICP source power.

Due to the strong chemical component of the Si etch process in fluorine based plasmas (the high volatility of the  $\text{SiF}_x$  etch products), etch rates are expected to increase with higher concentrations of  $\text{SF}_6$ . Si etch rates increased slightly as the  $\text{SF}_6$  flow rate increased from 60 to 120 sccm implying a reactant-limited etch regime at low flow rates. However at 150 sccm  $\text{SF}_6$  the etch rate decreased implying a diffusion-limited regime. The etch selectivity was typically < 50:1). Etch profile and morphology were essentially independent of  $\text{SF}_6$  flow rates.

#### *Aspect ratio dependent etching (ARDE) in DRIE*

The observation that smaller diameter vias and narrower trenches etch more slowly than larger diameter vias and wider trenches is often referred to as aspect ratio dependent etching (ARDE) or RIE lag.<sup>12</sup> An example of ARDE obtained in the DRIE process is shown in Figure 11 for 1 and 3.5  $\mu\text{m}$  wide trenches. The etch depth for the 1  $\mu\text{m}$  trenches was approximately 7.5  $\mu\text{m}$  while the 3.5  $\mu\text{m}$  trenches were etched to a depth of approximately 9.5  $\mu\text{m}$ . The difference in etch depth is attributed to transport of reactants and etch products into and out of the trenches.<sup>28</sup> As lateral dimensions decrease or the etch depths increase it becomes more difficult

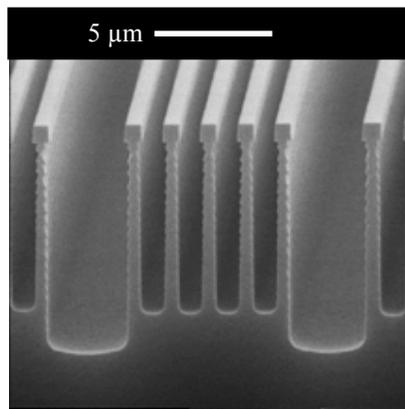


Figure 11. SEM micrograph of Si DRIE etch which demonstrates ARDE. The 1  $\mu\text{m}$  wide trenches were etched to an approximate depth of 7.5  $\mu\text{m}$  while the 3.5  $\mu\text{m}$  trenches were etched to a depth of approximately 9.5  $\mu\text{m}$ .

for the reactive species to diffuse to the bottom of the trench and more difficult for etch products to be extracted. Improved ARDE effects have been obtained for the DRIE process under high SF<sub>6</sub> flow conditions due to a reduction in redeposition of etch products.<sup>6,7</sup>

### *Etch selectivities*

Selective etching of one material over another is critical in the fabrication of many high-aspect ratio silicon structures. This is especially important for membrane-based devices (including FPW based-sensor devices, micro-valves, micro-heaters, bulk resonators, and accelerometers) where the etch process must stop on a thin film layer typically < 1 μm thick. Etch selectivities of Si to several films exposed to the DRIE process are shown in Table 1. DRIE etch conditions were 23 mTorr pressure, 100 sccm SF<sub>6</sub>, 40 sccm Ar, 850 W ICP source power, 8W cathode rf-power with a corresponding dc-bias of -25 to -50 V, and 20°C substrate temperature. As mentioned earlier, the high etch selectivity of Si to photoresist simplifies the process sequence for deep high-aspect ratio features by eliminating the need for hard masks. The high etch selectivities of Si to either SiO<sub>2</sub> or Si<sub>3</sub>N<sub>4</sub>, makes them excellent candidates for the membrane-based structures discussed below.

Material	Etch Rate (Å/min)	Selectivity to Si
Si	25,000	
Polysilicon	5334	4.7:1
LPCVD Silicon Nitride	295	85:1
PECVD Silicon Nitride	>1300	< 20:1
LPCVD SiO <sub>2</sub>	90	275:1
Thermal SiO <sub>2</sub>	90	275:1
LPCVD SiON	165	150:1
PECVD SiON	310	80:1
SiC (bulk)	140	180:1
Photoresist (AZ-4903)	250	100:1

Table 1. DRIE etch rates and selectivity to Si.

## **DRIE APPLICATIONS**

### *Chemical Sensing Devices*

The DRIE process has been applied to the fabrication of many integrated microsystems. One such group of integrated microsystems is chemical sensors and in particular the μChemLab integrated sensor.<sup>13</sup> This sensor consists of four major components; a) sample collection and concentration, b) chemical separation, c) detection, and d) an exit region. DRIE has been used in the fabrication of sample collection and concentration components as well as chemical separation components.

A pre-concentrator has been fabricated using the DRIE process to be used in the sample collection and concentration stage of the chemical sensor mentioned above.<sup>14</sup> The pre-concentrator is based on a membrane structure. A thermal SiO<sub>2</sub> or low stress, low pressure chemical vapor deposition (LPCVD) silicon nitride film is deposited on the frontside of a wafer. All frontside processing (metallization, etch, etc.) is completed and protected with a 3 to 5 μm layer of photoresist. The Si via etch mask is then applied on the backside of the Si wafer using a thick photoresist (~ 13 μm of Shipley 5740) and aligned to the frontside membrane features using backside alignment techniques. The wafer is then exposed to the DRIE etch process (where 400 to 685 μm of Si is removed) and etched to the SiO<sub>2</sub> or Si<sub>3</sub>N<sub>4</sub> membrane which is typically < 1 μm thick. The results of this process sequence are demonstrated in Figures 12 and 13. The SEM micrograph in Figure 12 shows a 400 μm wide Si via etched to a depth of approximately 685 μm at an etch rate of 3.5 μm/min. Due to the high etch selectivity of Si to SiO<sub>2</sub> (see Table 1), the DRIE process essentially stopped on the thermally deposited SiO<sub>2</sub> layer which was 0.6 μm thick. The via was highly anisotropic and maintained the dimensions of the mask, however the sidewall morphology was somewhat rough due to vertical striations and a slight Si foot was observed at the base of the sidewall. Ayon and co-workers have also observed a foot at the base of many of their features.<sup>6, 7</sup> They have been able to significantly reduce the foot dimensions by changing the deposition cycle of the DRIE process. The features observed at the bottom of the via in Figure 12b were frontside metal features which could be seen through the transparent thermal SiO<sub>2</sub> film. The SEM micrograph in Figure 13 shows a cross section of a DRIE through wafer via hole, which stopped on a silicon nitride membrane. The structure was used as a micro-hotplate using the frontside Pt-metal lines as the heater.

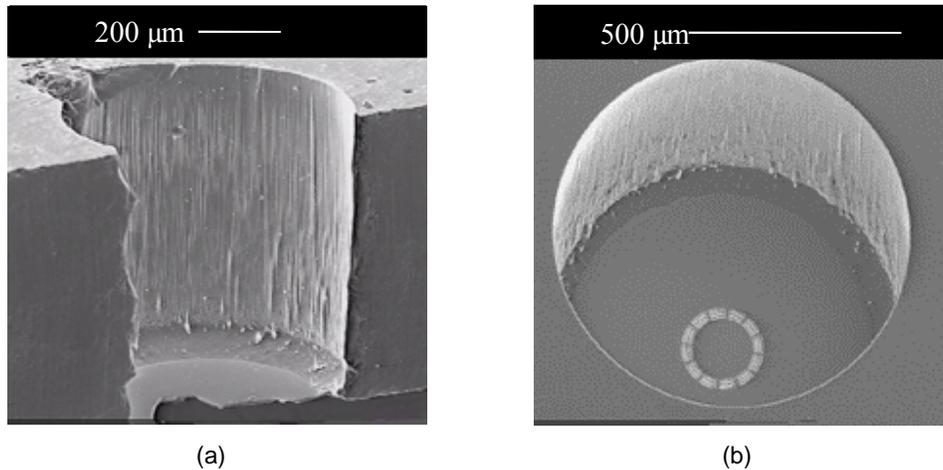


Figure 12. SEM micrographs of a Si via DRIE etched to a depth of approximately 685 μm to a 0.6 μm thick thermal SiO<sub>2</sub> layer which acts as an etch stop. The via diameter was approximately 400 μm.

In Figure 14, a packaged pre-concentrator containing 3 micro-heater membrane structures formed using DRIE is shown.<sup>13</sup> The center micro-heater was approximately 2.75 mm<sup>2</sup>, while the two smaller devices on either side were 0.5 mm<sup>2</sup>. Due to the highly anisotropic profiles obtained in the DRIE, as well as the ability to control the critical dimensions, the 3 micro-heaters were

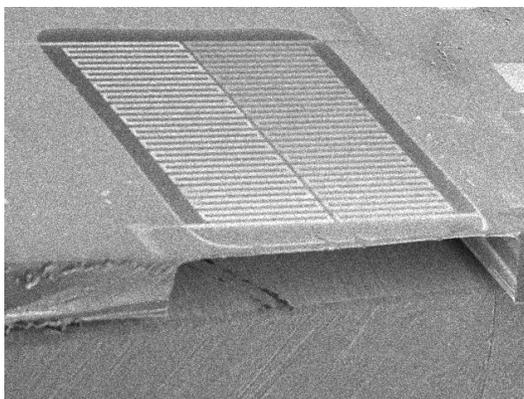


Figure 13. SEM micrograph cross section of a DRIE fabricated micro-hotplate. The frontside Pt heater lines are shown on top of the SiN membrane.

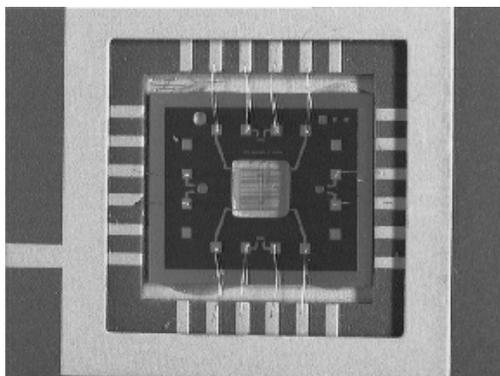


Figure 14. Photograph of a 24-PIN DIP packaged micro-hotplate die fabricated with the DRIE process. Temperature sensors are located on either side of the membrane device.

placed on independent membranes thus minimizing thermal cross talk and increasing thermal sensitivity. Fabrication of this device, using wet chemical etching, resulted in less efficient performance since the structures could not be closely spaced due to the crystallographic nature of the wet etch process. In Figure 15, the time response of a DRIE etched micro-heater to a square voltage pulse is shown. The device reached approximately 200°C in < 8 ms and 44 mW of applied power was necessary to obtain a stable output.

DRIE was also used to fabricate spiral micro-channels for open capillary tubing gas chromatographic (GC) separation.<sup>15</sup> Micro-channel devices have several advantages over more conventional GC structures including reduced size and cost, lower dead volume, and design flexibility. The performance of such devices is highly dependent upon optimization of channel length, width, and depth. Spiral micro-channels are etched into a Si substrate using DRIE. Following fabrication of the micro-channels a thin film was deposited over the micro-channels to form the stationary phase required for gas-phase separation. A Pyrex lid was then anodically bonded to the Si substrate to seal the micro-channels. Either stainless steel or glass capillary tubes were epoxied to the Pyrex lid to introduce and remove the gas from the micro-channel. A DRIE etched micro-channel is shown in Figure 16. The etch depth was approximately 240  $\mu\text{m}$  and the channels were 45  $\mu\text{m}$  wide. The spiral design was used to optimize channel length,

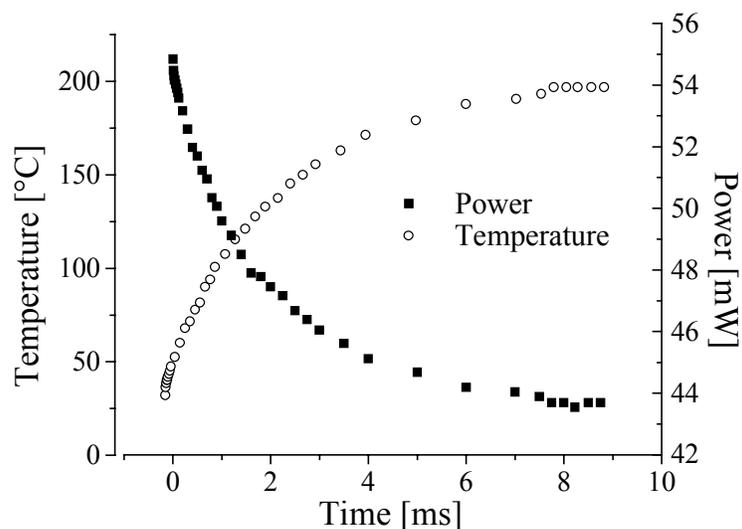


Figure 15. Time response of a 1 mm<sup>2</sup> micro-heater to a square voltage pulse.

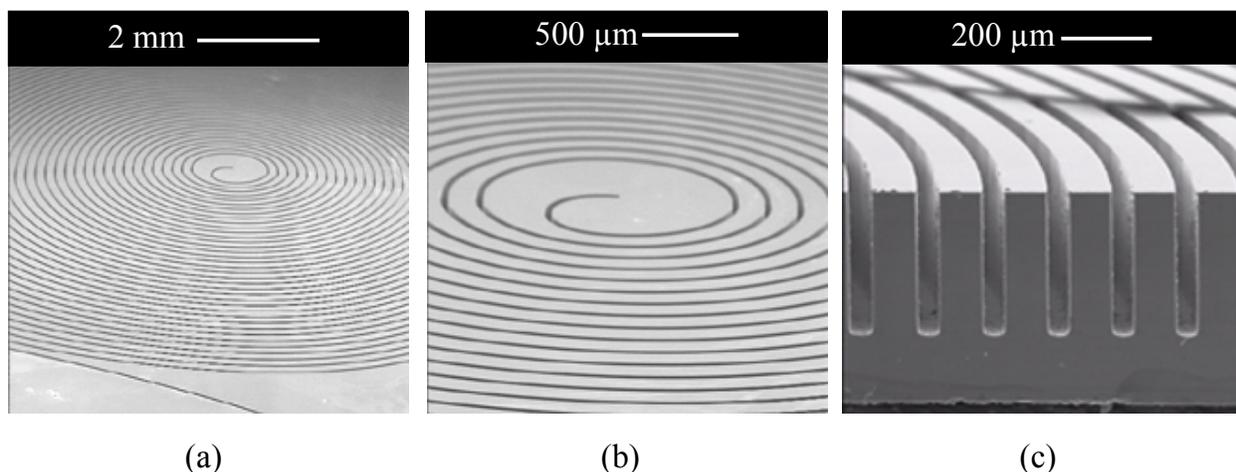


Figure 16. SEM micrograph of a GC micro-channel DRIE etched into a Si substrate. The channels were etched to a depth of 240 µm and were 45 µm wide.

while minimizing consumption of wafer real estate. Micro-channels have been fabricated with widths of 10 to 80 µm, depths of 150 to 330 µm, and lengths from 10 cm to 1 m. Figure 17 shows GC separation results for dimethyl methyl phosphonate (DMMP) from benzene, toluene, and xylene. The plot shows that these compounds can be effectively separated in a DRIE fabricated GC micro-channel in less than 1 minute.

Separation efficiency for either gas phase or liquid phase chromatography may be improved by optimization of the stationary phase coating or increased surface area within the micro-channel. Increased surface area can be obtained by etching high-aspect ratio Si features within the micro-channel. In Figure 18, 3 µm posts were etched in 100 µm wide micro-channels approximately 30 µm deep. The spacing was ~3 µm with an aspect ratio of ~10:1. The features were highly anisotropic and smooth with relatively high packing densities.

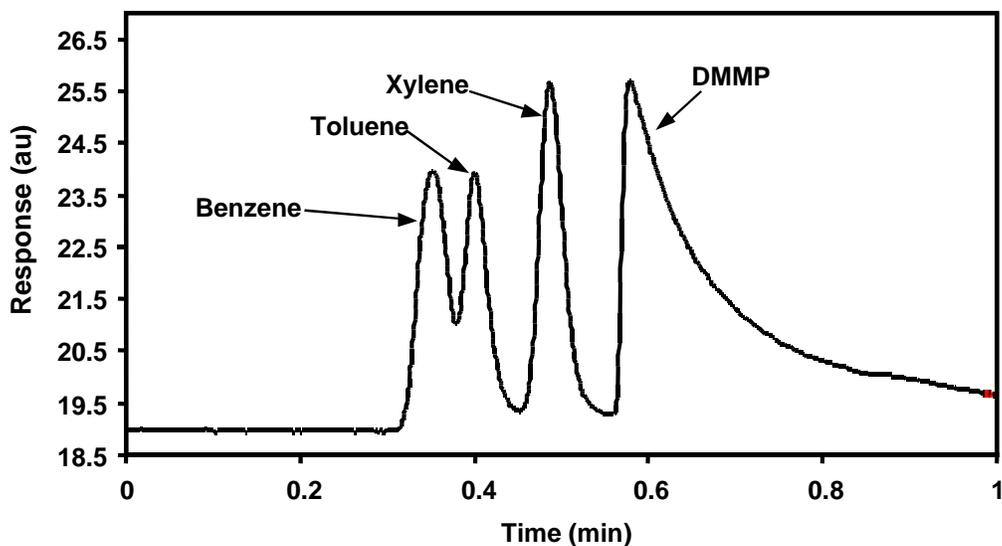


Figure 17. Separation of dimethyl methyl phosphonate from benzene, toluene, and xylene in a 1 m long, 40  $\mu\text{m}$  wide, 250  $\mu\text{m}$  deep DRIE etched GC micro-channel. The GC was operated at 40°C isothermal and a  $\text{N}_2$  carrier at 4 psi.

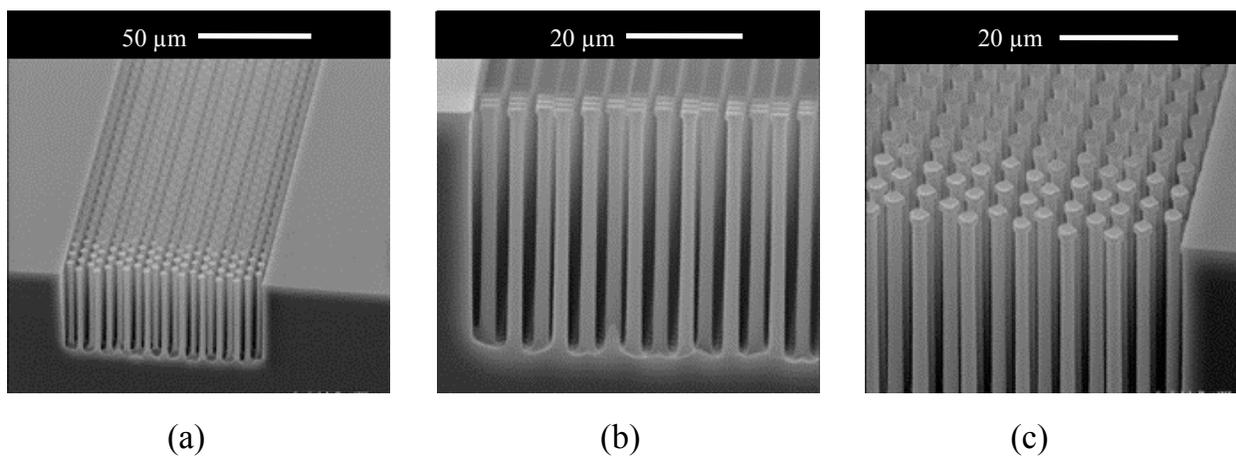


Figure 18. DRIE high-density, high-aspect ratio pins etched in a separation column to increase surface area. The features are 3  $\mu\text{m}$  diameter on 3  $\mu\text{m}$  pitch and etched to a depth of approximately 30  $\mu\text{m}$ .

#### Advanced Packaging

The DRIE process has also been used to accurately position discrete components onto Si substrates. Si substrates can be etched to multiple, specific depths while retaining accurately controlled dimensions in the mask plane. This permits accurate alignment of discrete components to one another. Thus, DRIE can be used to integrate a variety of microsystem components, with alignment tolerances  $< 10 \mu\text{m}$ . Figure 19 shows a schematic diagram of a Si substrate, which could be used for mixed technology integration and advanced packaging. For example, a well could be etched into the Si that could be used as a “device locator” to

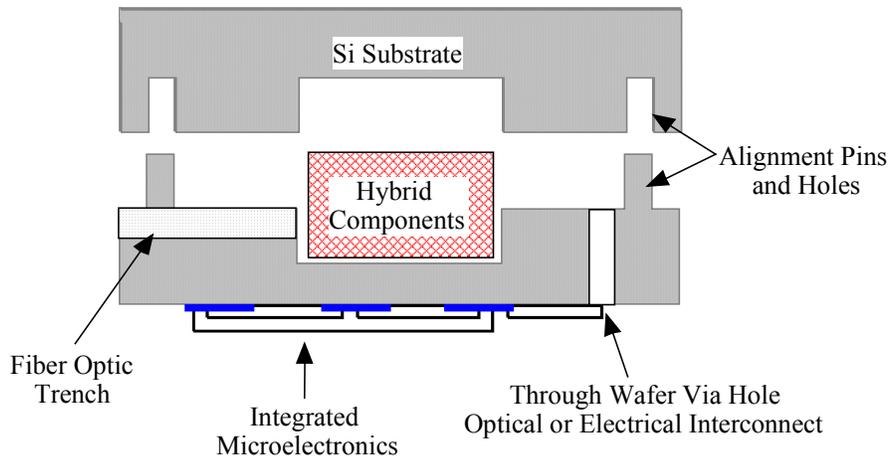


Figure 19 Schematic diagram of Si substrate used for advanced packaging of integrated microsystems. The DRIE process could be used to etch “device locators”, alignment pins and holes, trenches, and through-wafer vias for electrical or optical interconnects.

accurately position a hybrid device such as an edge-emitting laser or a vertical cavity surface emitting laser (VCSEL) onto the Si carrier. Using a second photolithography step, a trench could be etched into the Si to a precise depth and location relative to the laser in order to passively align an optical fiber. Also shown in the schematic are through-wafer via holes that could be used as either optical or electrical interconnects to frontside controlling and/or drive circuitry and a series of alignment pins and holes that could be used to accurately align multiple wafers for possible multi-chip-module (MCM) assemblies.

Several of these concepts are demonstrated in Figure 20 where a SEM micrograph shows Si features etched simultaneously to a depth of  $\sim 250 \mu\text{m}$ . In Figure 20a central square or “device locator” could be used to accurately position a hybrid structure while the trench features could be used for either electrical interconnects or extended to the edge of the wafer for an optical fiber. In Figures 20b and c, high magnification SEM micrographs show the high anisotropy, and smooth etch morphology of the sidewalls and the field. Vertical striations were observed in the sidewalls possibly due to striations in the photoresist mask which were transferred into the Si during the etch. It is also important to notice there is no sign of a foot or a fillet at the interface of the etched sidewall and field.

Wafer to wafer alignment has also been demonstrated using the DRIE process. In Figure 21, SEM micrographs show a)  $135 \mu\text{m}$  wide Si pins etched to a depth of  $\sim 360 \mu\text{m}$  and b)  $137 \mu\text{m}$  wide Si wells etched to a depth of  $400 \mu\text{m}$ . In Figure 21c, the pins are inserted into the well with a tolerance of  $\sim 4 \mu\text{m}$ . The Si samples were typically less than  $2.5 \text{ cm}^2$ .

A robust electroplated via technology has been developed and demonstrated for through-wafer electrical interconnects. The process includes a DRIE of Si to form the through wafer via holes. This is shown in Figure 22 for 100 and  $300 \mu\text{m}$  diameter vias in  $\sim 425 \mu\text{m}$  thick Si. The vias were then insulated with  $\sim 1 \mu\text{m}$  of  $\text{SiO}_2$  which was grown in a steam oxidation furnace at  $\sim 1050^\circ\text{C}$ . The vias were then electroplated using the following process. A copper plating fixture was coated with PMMA photoresist and solvent bonded to the Si wafer. The PMMA was patterned in an oxygen plasma using the Si via holes as a mask. The vias were then plated using

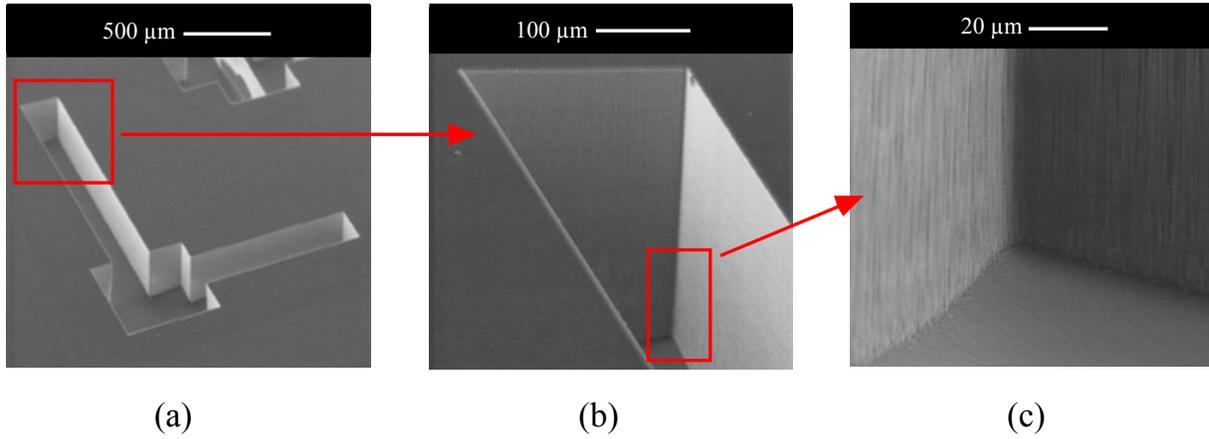


Figure 20. SEM micrograph of a device locator feature and 2 trenches for electrical or optical leads.

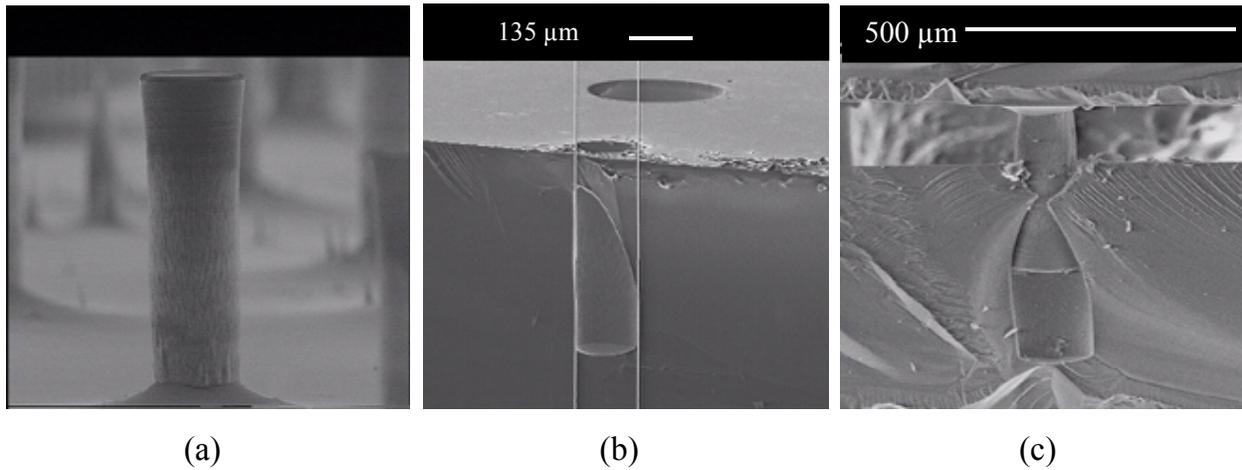


Figure 21. SEM of a) pins and b) wells for c) accurate wafer-to-wafer alignment. The alignment tolerance was approximately 4 μm.

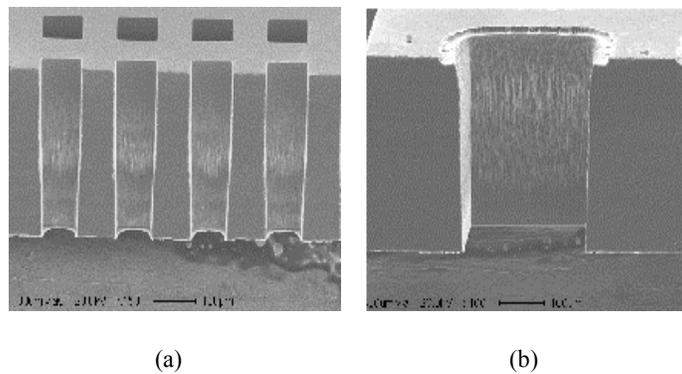


Figure 22. SEM micrographs of a) 100 μm and b) 300 μm diameter vias etched through a Si wafer using the DRIE process.

a Ni electroplating technology. Finally the copper plating fixture was removed in a wet etch process. Plated vias are shown in Figure 23 for 100 and 300  $\mu\text{m}$  diameter vias. A series of plated vias were tested electrically and determined to be isolated from the Si wafer. High voltage tests will be performed shortly.

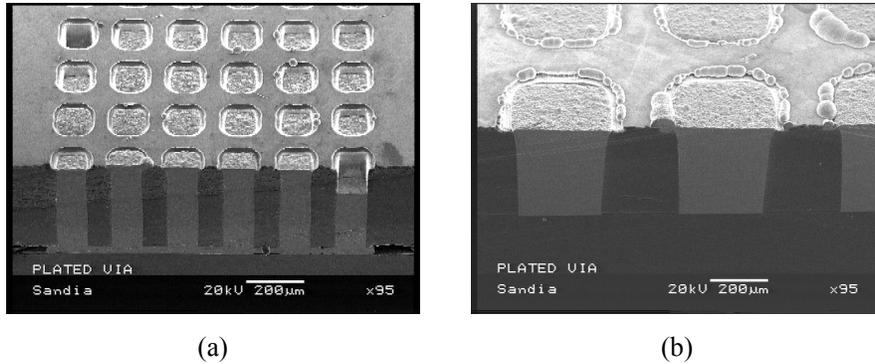


Figure 23. SEM micrographs of Ni electroplated Si vias for a) 100  $\mu\text{m}$  and b) 300 $\mu\text{m}$  diameter vias.

*Integration with LIGA*

By taking advantage of DRIE silicon etching, multi-level silicon alignment structures may be fabricated and used to assemble LIGA fabricated components. The results are shown in Figure 24 for a 450:1 torque-multiplying gear train that was designed and integrated onto a mask set incorporating various spacing and backlash configurations. The gear train used an array of 150  $\mu\text{m}$  diameter by 330  $\mu\text{m}$  tall pins, which were DRIE etched into a silicon wafer.

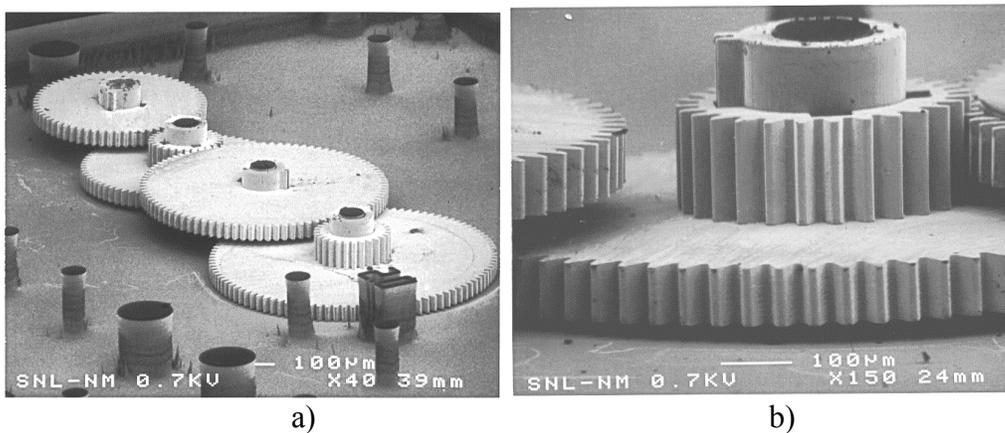


Figure 24. Two-level nickel gear train assembled into high aspect-ratio DRIE silicon etched substrate. The silicon pins are 150  $\mu\text{m}$  in diameter and 330  $\mu\text{m}$  tall.

A glass plate was bonded on top of the etched silicon die to provide for packaging during testing. The gear train was driven using an externally mated miniature (3mm diameter) brushless DC motor. The mechanism was run for several days indicating that silicon is a reasonable material to be used with metal LIGA components. These gear trains have been additionally coupled to linear racks and operated in the laboratory intermittently for several months.

This is the first step in demonstrating the use of silicon as a packaging material for LIGA components that allows the pursuit of further system integration. Integrated silicon microelectronics may be resident on the same assembly substrate and connected to the electromechanical assembly with electrical vias. Also, a complementary etched silicon substrate may be used to bond with the assembly substrate to serve as a cover and enable batch packaging.

Furthermore, the array of silicon assembly die provides a basis for batch assembly of LIGA components via wafer-to-wafer transfer and batch release. In this assembly sequence a silicon wafer is DRIE etched to form assembly geometry and alignment pegs. A complementary substrate with suitable sacrificial layer is fabricated with first level LIGA components, aligned to the silicon assembly substrate with which it engages, and finally a sacrificial etching step releases the components onto the assembly substrate. This batch assembly process has been successfully tested for one level and is expected to provide a technique suitable for multi-level LIGA batch assembly. More detail may be obtained from the publication "*Advances in LIGA-based post-mold fabrication*" which is included in this report.

#### *Post-processing of MEMS devices*

Integration of MEMS with optoelectronic components is a means of realizing miniature electro-optical and opto-mechanical subsystems that have great potential in weapon system and environmental sensor applications. A major obstacle to realizing these types of systems in a single structure is the difficulty of integrating the processing of the two classes of devices. The incompatibilities are due to dissimilar materials that have different processing temperature ranges and significant cross-contamination problems for a common process line. Another difficulty with direct integration of the two types of devices is providing the optical path for the MEMS components to interact with the light source. It is currently difficult to fabricate transparent optical components in conventional MEMS technology for use in the visible and near infrared portion of the spectrum. This limits the usefulness of simply stacking one device on top of another without a means of getting light through the MEMS substrate.

Realization of micro-optical systems required some additional capabilities in the processing of the MEMS devices. Because of incompatibilities with the processing line used for MEMS, these processes were developed at the CSRL in a "post processing" or "back-end-of-line" process relative to the MEMS process flow. One important requirement for implementing optical functions in MEMS is the ability to make good mirrors on the polysilicon surfaces. Both the shadow mask and lithographic metallization techniques discussed earlier have been demonstrated for this application. Some of the challenges included designing a process which would allow evaporation of Au on a previously released MEMS structure, without affecting its ability to move, obtaining good adhesion of the metal on surfaces coated with self-assembled monolayers (used to reduce stiction in MEMS devices), and minimizing the possibility of warp induced in the thin polysilicon structures upon evaporation due to stress caused by the metal film. These issues have been addressed and resolved. Figure 25 shows a) a shadowed masked Au metallized MEMS feature and b) a lithographically Au metallized MEMS pop-up mirror.

In addition, DRIE vias have been etched into MEMS structures for optical access. This was accomplished by first patterning temporary metal alignment marks on the front of the wafer and using backside alignment to pattern the via under the mirror. Vias were then etched using the DRIE process. One of the resulting vias is shown in Figure 26. These optical

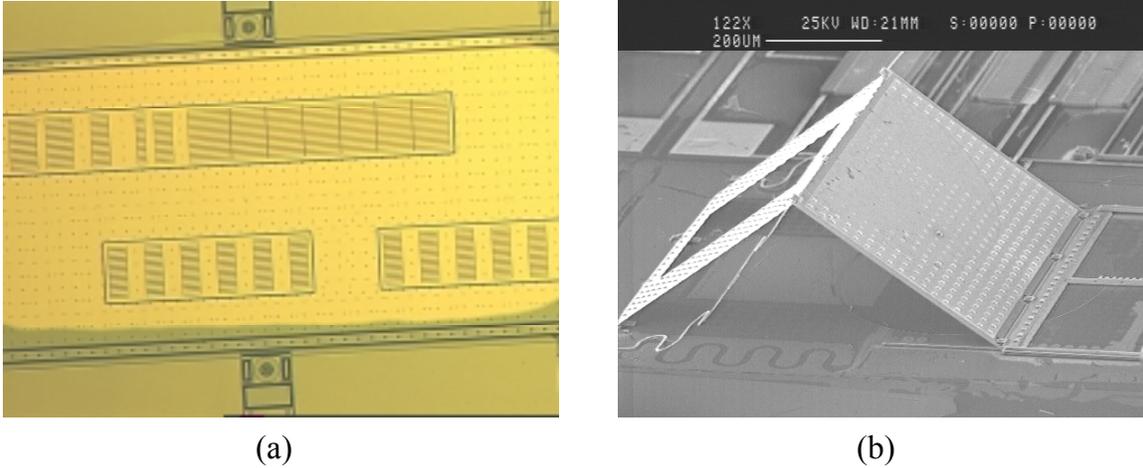


Figure 25. a) A shadowed masked Au metallized MEMS feature and b) a lithographically Au metallized MEMS pop-up mirror.

photomicrographs are taken from the backside of the wafer with illumination through the via. The backside of the mirror, and in particular the hinges are visible. This wafer was not yet been released and the via etch stopped on the  $\text{SiO}_2/\text{SiN}$  layer underneath the polysilicon layers comprising the MEMS structure.

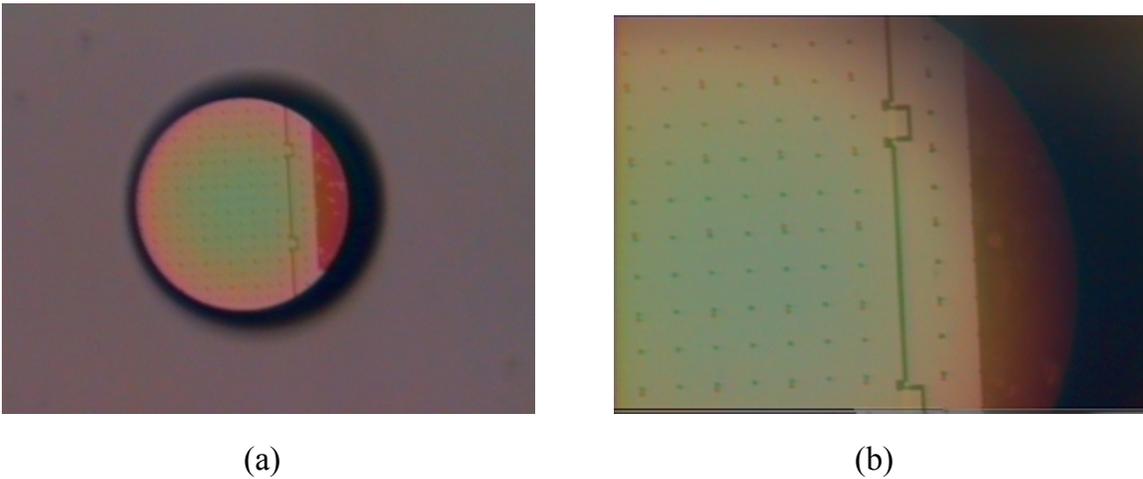


Figure 26. a) An optical microscope view of an DRIE etched via from the backside of a MEMS wafer. The unreleased polysilicon MEMS structure is visible in the bottom of the via. b) A magnified image of the MEMS structure which clearly shows the hinges of the poly-Si pop-up mirror.

Figure 27 shows a MEMS device mechanically shuttering the beam from a VCSEL. In order to ensure opaqueness to the VCSEL incident beam, gold was evaporated on the top surface of the mechanical shutter. A DRIE via has been etched in the Si MEMS wafer and is aligned to the VCSEL. In Figure 27b, the VCSEL light is visible through a hole in the gold-covered MEMS shutter. As drive voltages are applied to the electrostatic micro-motor, the shutter rotates, thus

periodically allowing the VCSEL to transmit through the device. Depending on the control signals, the shutter can rotate in either direction and at a variety of speeds. By thus blocking or passing a laser beam, the MEMS shutter can be used to enable transfer of signals or power by optical means.

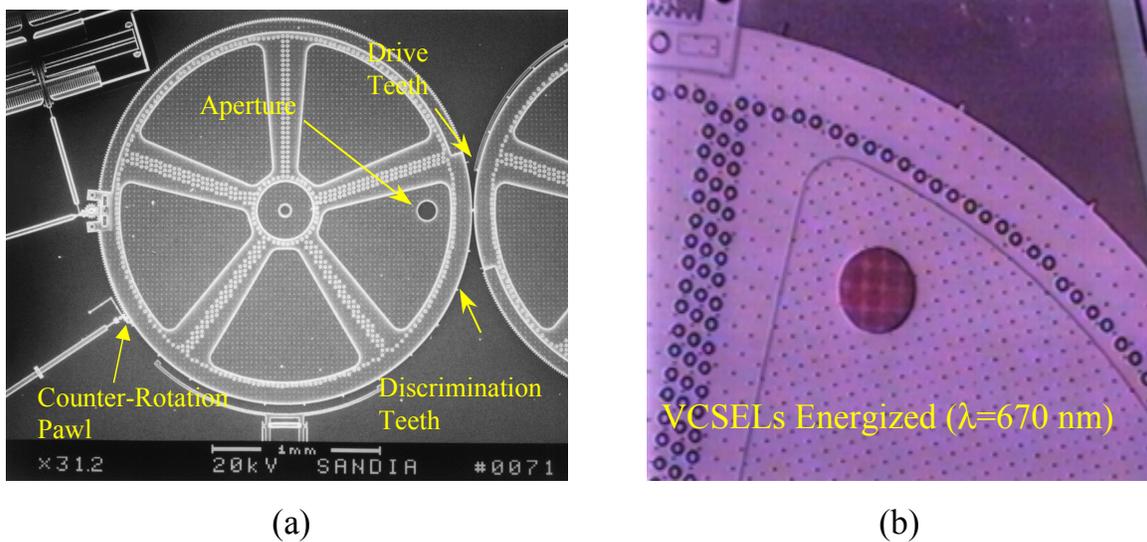


Figure 27. Top view of the a) metallized shutter and b) a VCSEL beam visible through a hole in that shutter.

Post-processing DRIE has also been applied to the fabrication of microfluidic devices (see Figure 28). These devices can be fabricated using a wide range of technologies including bulk micromachining (e.g. KOH etch), high aspect ratio micromachining (e.g. DRIE or LIGA), laser machining, very small scale conventional machining (drilling and milling), and capillary tubing assembly. However, surface micromachining of such devices has not been utilized. Surface micromachining has significant potential advantages over other fabrication techniques in some microfluidic applications. One advantage is volume minimization. A typical bulk micromachined microfluidic device has a channel depth on the order of 100  $\mu\text{m}$  and a volume on the order of 100 nl (assuming an approximately 500  $\mu\text{m}$  wide by 1 mm long channel). A typical surface micromachined channel is only 2 to 5  $\mu\text{m}$  deep, 200  $\mu\text{m}$  wide and 1 mm long for a volume on the order of 1 nl (2 orders of magnitude smaller). In applications where volume minimization is important this difference could be significant in reducing mixing times and reagent requirements. Microfluidic channels have been fabricated in the MDL using either silicon nitride membranes or as polysilicon MEMS structures. In order to introduce fluid at the channel inlet and outlet, vias were etched through the wafers from the backside using the DRIE process. The DRIE etched via extended all the way through the wafer and stopped on the nitride layer at the bottom of the channels. The vias were 200  $\mu\text{m}$  in diameter. Finally the nitride membrane on the bottom of the channel was removed using a parallel plate RIE system. More details of this work is available in Appendix A “*Surface Micromachine Microfluidics: Design, Fabrication, Packaging, and Characterization*” which is included in this report.

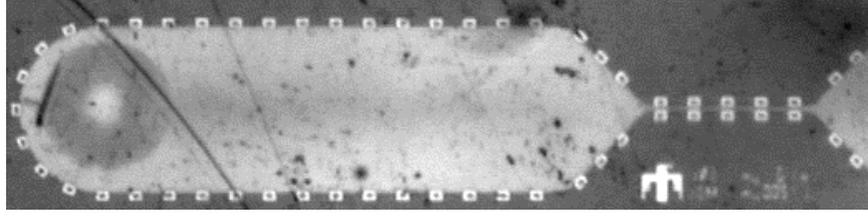


Figure 28. Photograph of a micro-fluidic channel. The etch release holes are spaced around the channel edge. The channel necks down to 10  $\mu\text{m}$  in width at the left and is 200  $\mu\text{m}$  wide where the Bosch etch hole intersects the channel at the left.

## FLEXURAL PLATE WAVE SENSOR DEVELOPMENT

### *Flexural Plate Wave Device Description and Operation*

One of the sensor platforms pursued in this project involves excitation of acoustic waves in a bounded, thin membrane as the sensing mechanism. These acoustic waves are called flexural plate waves (FPWs). FPWs penetrate the entire thickness of the thin membrane rather than just the surface region of a bulk substrate like the surface acoustic waves (SAWs) used in other platforms pursued in this project. FPWs can be excited with piezoelectric thin films (ZnO, AlN, or lead-titanate materials), or as in the present program, via the Lorentz force interaction between an ac current and a fixed magnetic field. Lorentz force excitation eliminates many of the processing and integration difficulties associated with the piezoelectric thin film materials.<sup>16</sup>

The operation of the mag-FPW resonator has been described in detail in Reference 16 and is illustrated in Figure 29. The device is formed by (1) depositing a low-stress silicon-nitride (SiN) layer on both sides of a <100> silicon substrate, (2) patterning a square or rectangular opening in the backside SiN layer, (3) patterning a meander-line current conductor on the front surface SiN layer (centered with respect to the rectangular opening on the backside), and (4) performing an anisotropic silicon etch to remove the silicon below the membrane. This leaves a precisely sized, freestanding rectangular membrane held within a silicon frame and current lines positioned to preferentially excite a selected membrane mode.

Current lines, running across the width of the membrane, are positioned at regular intervals on the insulating membrane surface. When a static, in-plane magnetic field is applied perpendicular to the current direction, a surface-normal Lorentz stress (force per area)  $\vec{F}$  is generated:

$$\vec{F} = \vec{J} \times \vec{B} \quad (1)$$

where  $\mathbf{J}$  is the two-dimensional current density on the membrane surface and  $\mathbf{B}$  is the magnetic flux density. The reversing current direction between successive legs in the meander-line transducer (MLT) generates spatially alternating surface-normal Lorentz forces ( $F_z = B_x J_y$ ). Proper positioning of these current lines with respect to the membrane boundaries allows excitation of an eigenmode of the rectangular membrane.

The MLT serves to detect membrane resonances as well as excite them. In a one-port device, motion of the MLT in the magnetic field generates an impedance change that can be used to track membrane resonance: an electromotive force (emf) is induced due to motion of the

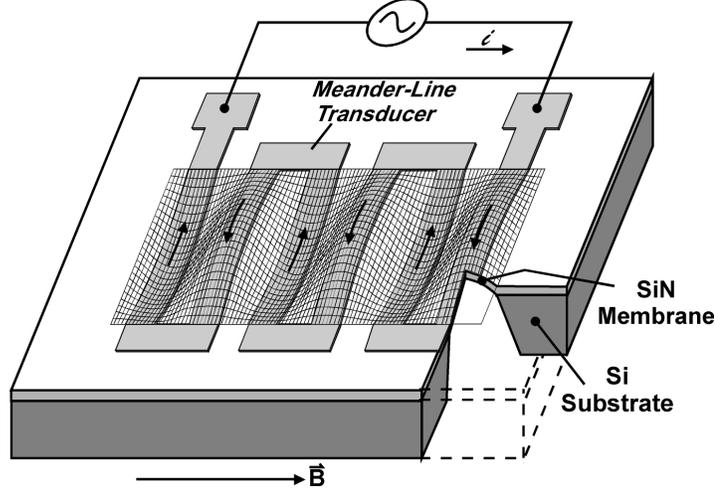


Figure 29. Schematic representation of a one-port, mag-FPW resonator. The acoustic wave is excited by the interaction of the static magnetic field  $B$  and the alternating current  $i$ , via the Lorentz force. At any instant in time, the current direction alternates from one leg to the next in the meander-line transducer, causing Lorentz forces in opposite directions. The wavelength of the meander line transducer (MLT) and its position on the bounded SiN membrane cause preferential excitation of a particular vibrational mode.

conductor in the magnetic field. In a two-port device, the membrane resonance excited by forcing an ac current in a first (input) transducer produces motion that generates a voltage on a second (output) transducer.

Referring to the geometry of Figure 29, the surface-normal membrane displacement  $u$  generated by the distributed Lorentz force is determined by:<sup>17</sup>

$$D \Delta^4 u - T \Delta^2 u + Z_a \dot{u} + \rho_s \ddot{u} = -B_x J_y \quad (2)$$

where  $D$ ,  $T$ , and  $\rho_s$  are the membrane bending moment, tension (force per edge length), and areal mass density, respectively;  $Z_a$  is a mechanical impedance arising from fluid loading (gas or liquid). The bending moment  $D = Eh_1^3/[12(1 - \nu^2)]$ , where  $E$  is Young's modulus,  $\nu$  is Poisson's ratio, and  $h_1$  is the membrane thickness. Internal membrane damping can be included by using a complex Young's modulus  $E^* = E(1 + j\delta)$ , where  $\delta$  is the loss tangent, to calculate the bending moment.<sup>18</sup> Solutions for two limits of this equation are described in Reference 16: linear solutions that apply for small-amplitude oscillations; and nonlinear solutions for larger amplitude oscillations. The linear response model is sufficient for the purposes of the present discussion.

In the linear response model, a rectangular membrane supported at the edges can be excited into a number of eigenmodes. Provided the membrane is thin compared to an acoustic wavelength, these eigenmodes can be found analytically in the linear regime, with displacement given as a superposition of normal modes:<sup>19</sup>

$$u(x, y, t) = \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} A_{mn} \sin(k_m x) \sin(k_n y) e^{j\omega t} \quad (3)$$

where  $A_{mn}$  is the complex displacement amplitude of the  $(m,n)$  eigenmode;  $k_m = m\pi/l$  and  $k_n = n\pi/w$ , where  $l$  and  $w$  are the membrane length and width, respectively, and  $m$  and  $n$  are integers denoting the longitudinal (in the  $x$ -direction) and transverse ( $y$ -direction) mode variations;  $\omega = 2\pi f$ , where  $f$  is the excitation frequency. Figure 29 shows the membrane being excited into an  $m=6, n=1$  mode.

Membrane resonances (in vacuum) occur at excitation frequencies given by Eq. 4.<sup>16</sup> In a fluid, the frequency will be shifted due to the fluid loading on the membrane. At resonance, membrane displacement is maximized, limited only by fluid loading and internal membrane damping.

$$\omega_{mn} = k_{mn} \left( \frac{D k_{mn}^2 + T}{\rho_s} \right)^{\frac{1}{2}}. \quad (4)$$

Equation 4 describes all of the possible resonance modes of the rectangular plate. However, the MLT is designed to preferentially excite a particular membrane mode. The edges of the clamped membrane define nodes in both the longitudinal and transverse modes. Efficient coupling to a particular longitudinal (index  $m$ ) mode can be achieved by positioning current lines along the longitudinal mode maxima, i.e., centered at  $[\lambda/4 + p(\lambda/2)]$  relative to the edge of the membrane, where  $\lambda$  is the longitudinal mode wavelength and  $p$  is an integer. The MLT couples most efficiently to the longitudinal mode with the same periodicity. When the current lines extend across the width of the membrane, as pictured in Figure 29, the Lorentz force is uniform across the membrane in the transverse direction and does not match the fundamental transverse mode profile. The uniform transverse force distribution couples to a family of odd-order transverse modes ( $n=1,3,5,\dots$ ), with coupling strength varying as  $1/n$ .

As mentioned above, a single longitudinal  $m$ -mode can be preferentially excited by proper positioning of current lines on the antinodes for this mode. The associated  $n = 1$  (transverse) mode should be excited most efficiently and can be targeted for use. When exciting the device over a narrow frequency range near this isolated mode, the device model can be simplified by using only the single term in the summations that corresponds to this mode. In practice of course, processing and alignment imperfections limit the efficiency of coupling to the target mode, and also allow excitation of other modes with sufficiently close resonant frequencies.

Examination of Eq. 4 indicates that the resonant frequency of the mag-FPW is determined by the MLT design (i.e., the target wavelength chosen based on the membrane dimensions), the bending moment  $D$  of the composite membrane, the membrane tension per edge length  $T$ , and the areal mass density  $\rho_s$ . With no external stimuli, the tension  $T$  is determined by the residual stress in the composite membrane made up of the SiN and the metal conductor lines. These materials also determine the areal density.

The tension and areal density of the membrane dominate the resonant frequency of the mag-FPW devices used in this program. (That is, in Eq. 4,  $T_0/(Dk_{mn}^2) \gg 1$ .) When using the FPW device as a sensor, any stimulus affecting these two parameters can be detected.

### FPW Fabrication Process

We have used two basic methods to fabricate mag-FPW devices. An anisotropic silicon etch is used in both methods, but in one case it is a wet etch (hot KOH solution), and in the other the DRIE process is used. At the beginning of this project the wet etch method was all that we had used. The simpler, dry etch process was the main focus for FPW devices in this work because it is the process of choice for future post-processed, fully integrated mag-FPW sensor systems. Both processes are described here so that the stringent requirements for the DRIE FPW process are clearly highlighted.

The major steps in the wet-etch fabrication process for mag-FPW devices are depicted in Figure 30. A (100) silicon wafer, polished on both sides, is coated on both sides with a low-stress silicon nitride layer. This layer is deposited using LPCVD at about 830°C. On the front side, this layer will act as the dielectric FPW membrane. On the backside, it will act as a mask for the anisotropic Si etch. A photoresist layer is then patterned on the backside to define the openings for the FPW membranes. These openings must be precisely aligned to the  $\langle 110 \rangle$  planes of the Si wafer<sup>20</sup> because the subsequent anisotropic Si etch will naturally align the membrane edges to these directions (the etch rate on  $\langle 111 \rangle$  planes is dramatically lower). Misalignment of these openings to the  $\langle 110 \rangle$  planes causes the membrane to be larger than intended and the transducers to be misaligned with respect to the membrane. Both of these effects make the device less efficient in exciting the intended resonant mode discussed above. A separate etch step is used to accurately indicate the crystal planes since the normal alignment

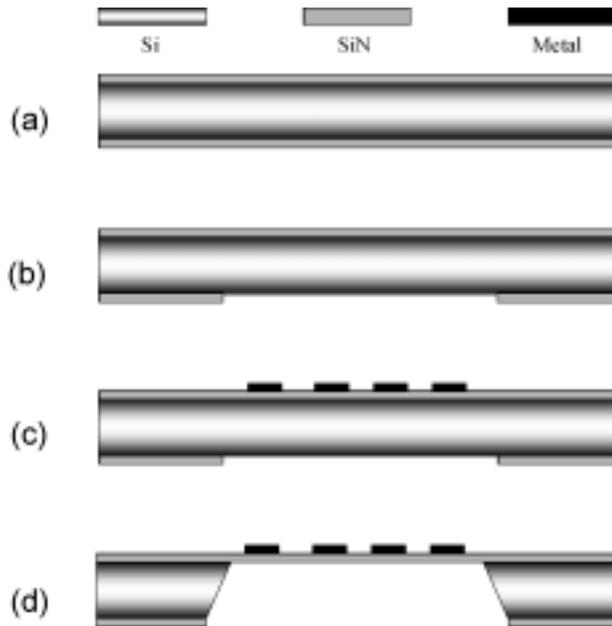


Figure 30. Cross sectional representations after key steps in the fabrication of mag-FPW resonators using hot KOH solution as the anisotropic silicon etch. (a) The starting substrate is coated on both sides with low-stress SiN. (b) Patterned photoresist and a dry etch are used to open the etch window in the backside SiN (these windows must be precisely aligned to the  $\langle 110 \rangle$  directions on the  $\langle 100 \rangle$  silicon wafer). (c) Metal is patterned on the front side, with the resulting MLT centered with respect to the window on the backside. (d) The membrane is released using an anisotropic wet etch (hot KOH solution).

accuracy of the wafer flat is not sufficient. The photoresist openings for the membrane etch must also be larger than the intended membrane size to account for the  $54.7^\circ$  angle of the  $\langle 111 \rangle$  planes left behind by the wet etch. A dry etch is used to remove the SiN from the windows patterned in the photoresist layer. Next the metal MLTs are patterned on the front side of the wafer. Double-sided alignment is used to ensure proper positioning of the MLTs with respect to the eventual FPW membranes so that the proper mode will be excited. Aluminum metallization was used in the mag-FPW devices fabricated in this project. The final step is to release the FPW membranes using the anisotropic Si etch ( $85^\circ\text{C}$ , 35% KOH solution). Since the aluminum is attacked by the KOH solution, the front side is protected by Apiezon black wax during the KOH etch. Successive rinses in trichloroethylene, acetone, and methanol are used to remove the black wax after the Si is completely removed from beneath the FPW membrane.

It is apparent that the above anisotropic wet etch process is not very compatible with post-processing of FPW devices on smart substrates. This was the impetus behind developing an FPW process based on the DRIE process. The dry etch does not require immersion of the smart substrate into a hostile etch bath that would damage much of the circuitry. The DRIE is also not restricted to particular crystal planes; arbitrary shapes can be etched at any angle.

Thus the DRIE process for the FPW device is considerably simpler than the wet-etch process. The key characteristic of the DRIE is the high selectivity for preferentially etching Si with respect to photoresist ( $\sim 100:1$ ), thermal or LPCVD  $\text{SiO}_2$  ( $\sim 275:1$ ), or low-stress LPCVD SiN ( $\sim 85:1$ ). Appropriate thicknesses of these materials (or combinations of them) can thus be used to define structures formed using the DRIE process. In principle, the DRIE process results in vertical sidewalls, allowing closer spacing of structures, and more freedom in the type of geometric structures that can be formed. Key stages in the typical one-step DRIE processing sequence for FPW devices are shown in Figure 31. A silicon wafer [can be any orientation, but is normally (100)], polished on both sides, is coated on the front side with a low-stress silicon nitride layer (this coating is not required, but can be tolerated on the backside). MLTs are patterned on the front side of the wafer. DRIE etch windows are then patterned in a thick photoresist layer on the backside of the wafer. These windows must be precisely aligned with respect to the MLTs on the front side. The DRIE etch is then used to remove the silicon and release the membrane.

Unfortunately, the one-step DRIE process did not yield the dimensional accuracy needed for the FPW resonators. Figure 32 shows an optical micrograph of a typical silicon "foot" left behind by the one-step DRIE process. In this particular device the foot is a few hundred microns wide, but not particularly uniform around the perimeter. Typically the foot characteristics are also not uniform across a wafer, making it difficult to compensate for them in the design. The foot width is reduced with continued etching, but the edges begin to balloon out from the intended location. Furthermore, the etch continually attacks the nitride membrane, leading to non-uniform thickness, or even complete removal. Even if one minimizes the damage to the membrane with an oxide etch stop for better selectivity, simple overetching cannot provide the needed dimensional accuracy.

We were not able to solve the above non-uniformity problems by simply optimizing the etch process through the various control parameters. Therefore we attacked the problem with a two-step etch process which is depicted in Figure 33. The additional steps shown in Figure 33 are inserted immediately after step C in Figure 31. The initial layer on the back of the wafer is now called a "hard mask." This could mean an oxide, nitride layer patterned by wet chemical or dry etch, or a photoresist layer that is hard baked after patterning. In any of these cases, the hard

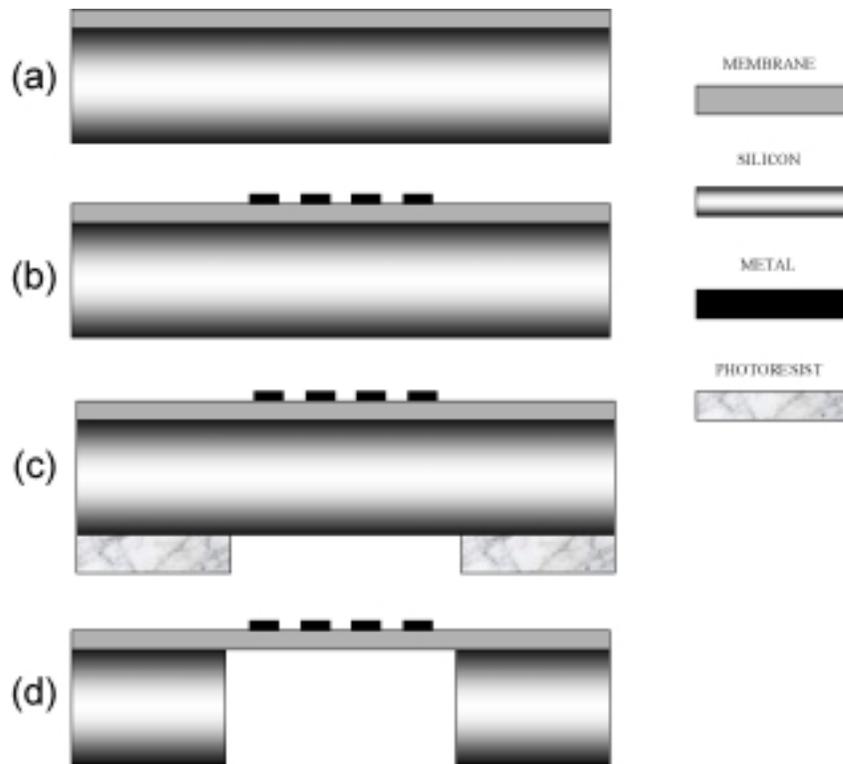


Figure 31. Cross sectional representations of key steps in the fabrication of mag-FPW resonators using a one-step, dry, DRIE etch as the anisotropic silicon etch. (a) The starting substrate is coated on the front side with low-stress SiN (or another suitable membrane material). (b) Metal is patterned on the front side to form the MLT (no alignment to crystal planes is necessary). (c) Patterned photoresist defines a window on the backside that is centered with respect to the MLT already defined on the front side. (d) The membrane is released using the Bosch etch (ideally this etch forms vertical sidewalls).

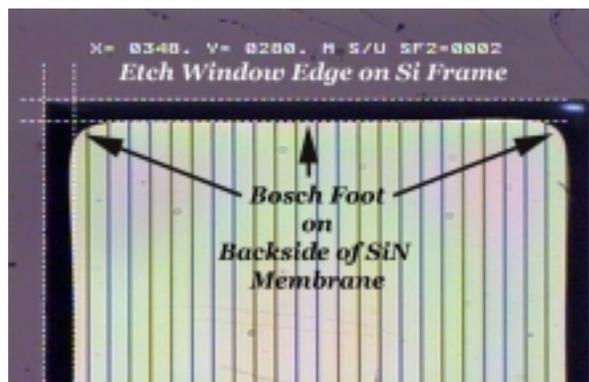


Figure 32. Optical micrograph depicting the typical Si "foot" remaining when a one-step DRIE is used to release the FPW membrane. The intended edge of the membrane is the outside edge of the darker region.

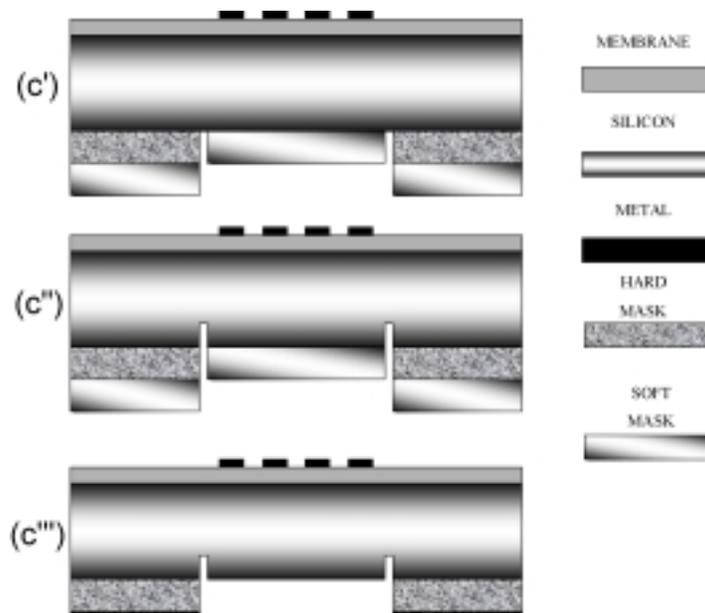


Figure 33. Additional steps used in implementing a two-step DRIE that provides vastly improved dimensional control for the FPW membrane. The patterned resist in step C of Figure 31 is hard baked and then protected with a normal soft baked resist that also protects the center region of the membrane etch window. The narrow channel (50 $\mu$ m wide) around the perimeter of the membrane is etched partway into the wafer as depicted in panel c'' (normally about 25% of the wafer thickness). Then the soft mask is stripped and the etch is run until the membrane is released.

mask must be of sufficient thickness to allow complete release of the frontside membrane. After patterning the hard mask, a soft mask photoresist layer is patterned that protects not only the hard mask, but also the center region of the membrane. This defines a narrow “channel” around the perimeter of the FPW membrane that is etched into the wafer. After giving the “channel” a sufficient head start, the soft mask is removed and the DRIE is run to completion using the hard mask. By carefully choosing the width and depth of the head start “channel” we were able to clear the entire membrane almost at once, with a foot that was less than half the width of the channel. Since the silicon etch proceeds more slowly in the narrow channel around the perimeter than it does in the large membrane area we can take advantage of the ARDE or RIE lag effect. The RIE lag effect is shown in Figure 34. The hard mask was an oxide layer in the device shown here, but we have also demonstrated the technique with hard-baked photoresist.

Figure 35 shows that the two-step DRIE process provides dramatic improvement in the dimensional control of the FPW device. The early DRIE-etched devices displayed an irregular silicon foot that could be several hundred microns wide and quite variable across a wafer (see panels (a) and (b) of Figure 35). The two-step DRIE process is more repeatable and uniform across the wafer, and results in a regular foot of a only a few microns (panels (c) and (d) of Figure 35). Figure 36 compares the appearance from the front side of a two-step DRIE-processed FPW resonator with a KOH-etched device. The key thing to notice is the curvature in the DRIE etched membrane edge as compared to the KOH membrane edge defined by the  $\langle 111 \rangle$

crystal planes. However, the repeatability, uniformity, and elimination of the silicon foot make it possible to compensate in the mask design for the remaining process-related imperfections.

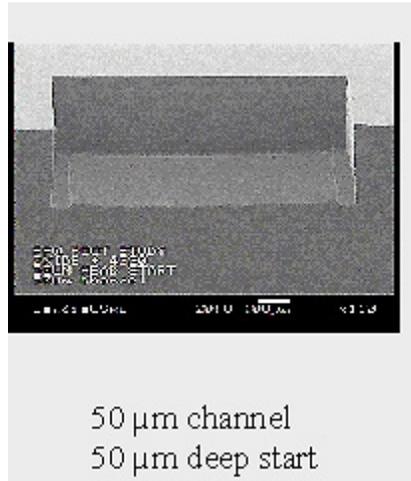


Figure 34. Optical micrograph showing the effects of ARDE or RIE lag. The initial head start channel was 50  $\mu\text{m}$  wide and etched 50  $\mu\text{m}$  deep. The soft mask was then removed and this picture was taken after etching 225  $\mu\text{m}$ . It is clear that the center region is catching up with the channel region. In general, we have found that the head start etch should be about 25% of the final

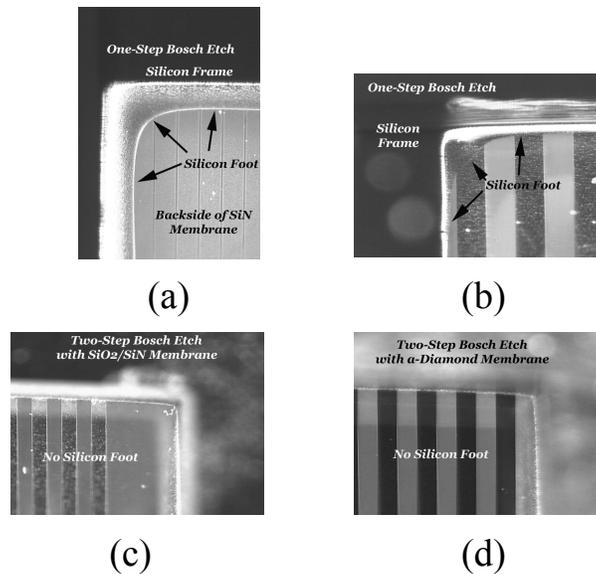


Figure 35. Optical micrographs highlighting the improved control over the silicon foot left behind by the one-step DRIE process. Panels (a) and (b) show typical results with the one-step etch when using SiN membranes. Panels (c) and (d) show the vertical sidewalls achieved with the two-step process, and the lack of a silicon foot. The corners of the membrane are still slightly rounded (25- $\mu\text{m}$  radius is typical) and the edges slightly bowed. The rounded corners

are not critical and the bowed membrane edge can be compensated in the mask design to give a sufficiently straight edge.

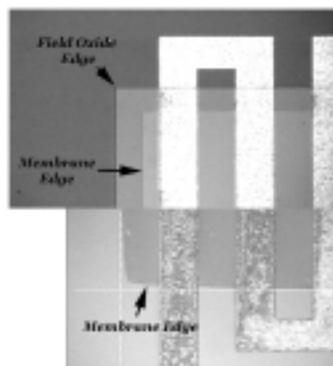


Figure 36. Optical micrographs of the corner of FPW resonator membranes released with either a KOH etch (top panel), or the two-step DRIE etch (lower panel). These pictures are taken from the front side of the membrane (see panels (c) and (d) of Figure 35 for the appearance from the backside of the DRIE-etched membrane).

We have successfully demonstrated the use of DRIE-processed FPW resonators as chemical sensors to illustrate the feasibility of the process for this sensor platform. Figure 37 shows the results of xylene vapor detection with a dual membrane FPW resonator. One membrane (uncoated) acts as a reference, while the other (coated in this case with ethyl cellulose), acts as the detector. The sensitivity of a few parts per million with no preconcentration makes this technology competitive with surface acoustic wave sensors used in Sandia's  $\mu$ ChemLab project. The DRIE process could easily fabricate an array of several

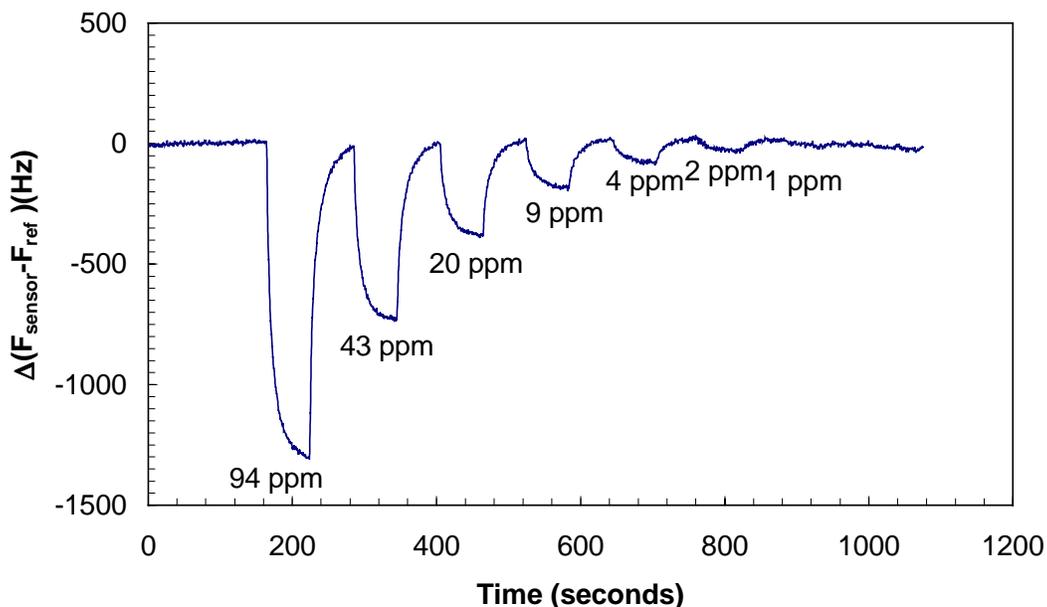


Figure 37. Response of a dual-membrane FPW chemical detector to 60-second xylene challenges of the concentrations indicated. The uncoated reference membrane is used to compensate for drifts in ambient conditions, while the detector membrane (coated with ethyl

cellulose in this case) responds to the analyte challenge. These tests were done with no preconcentration of the analyte vapor.

membranes on the same chip to enable the use of several different sensor coatings for increased discrimination between a variety of analytes.

### ***FPW Membranes for Post-Processing***

The eventual goal for mag-FPW technology is to take advantage of its process compatibility with silicon microelectronics and move to full integration of the drive electronics on a smart substrate with the sensor itself. This would lead to a very capable and versatile sensor platform. In this scenario, the mag-FPW sensor would be post-processed in vacant real estate saved for this purpose on the smart substrate with the ASIC drive electronics already completed. This places certain requirements on the membrane material of the FPW resonator. The membrane layer must either be able to withstand the processing of the smart substrate without degradation of its critical characteristics (residual stress), or be capable of deposition after processing of the smart substrate. In the former case the membrane must withstand the thermal processing used in fabricating the integrated drive electronics. This may involve temperatures up to 1000°C and higher. In the later case, the metallization of the finished drive electronics limits the highest temperature that can be used in the processing of the membrane layer to about 450°C.

The favored membrane material to date for the FPW devices has been low-stress, LPCVD SiN. This material is deposited in an almost stress-free state at about 830 to 860°C that is too high to allow SiN deposition on the finished ASIC wafer. However, standard ASIC fabrication following the LPCVD SiN deposition is not expected to degrade the film. Therefore post-processing for FPW sensors appears feasible.

Amorphous, diamond-like carbon (a-D) membranes have shown promise for FPW sensors. These films show remarkable etch selectivity with respect to silicon in the DRIE process. We have successfully fabricated FPW devices using this material at thicknesses ranging from 0.25 to 1.5  $\mu\text{m}$ . The chemical sensing results shown in Figure 37 were obtained with an a-D membrane device. Unfortunately, a-D films require a 600°C stress relief anneal, which is too hot for post-processing. Furthermore, exposure to temperatures above 600°C causes dramatic increases in the tensile stress, making the material unsuitable for freestanding membranes. Therefore, a-D membranes are suitable only for hybrid integration with the smart substrate.

We have considered and investigated several other potential membrane materials for post-processing. According to the literature, plasma enhanced chemical vapor deposited (PECVD) low-stress SiN or SiC membranes should be possible. However, with the equipment we have available in the CSRL, we have not been able to simultaneously achieve the needed combination of low residual tensile stress, etch selectivity, and absence of pinholes.

Late in the course of this project we started investigating potential polymer films for post-processing as FPW membranes. The two most promising candidates appear to be Cyclotene from Dow Chemical and polyimide materials available from a variety of manufacturers. Both types can be obtained in photosensitive versions, are processed at temperatures below 300°C, and can form low residual tensile stress layers if properly processed. Whether these polymer materials will be suitable for all of the potential applications remains to be seen. In particular, they may lead to unacceptable "memory" effects in chemical sensing applications due to solubility of analyte vapors. Development at Sandia of the polymer membrane materials for post-processing of FPW devices is continuing as part of other sensor development projects.

### FPW Oscillator Circuitry

The FPW oscillator block diagram is shown in Figure 38. One of the main design requirements is that the sensor-system operates at low power. Another design constraint was that the power dissipated by the FPW must be kept to a minimum. This is due to FPW nonlinearities and power dissipation capability. If the FPW is driven too hard it can be catastrophically damaged due to the large EM forces on the FPW conductors. This design operates the FPW at approximately 0.2 mW, assuming a  $15\Omega$  impedance. This oscillator comprises four main functions ( $A_1$ - $A_4$ ) plus the FPW sensor. Due to multiple design constraints a custom (non-op amp) design was developed.

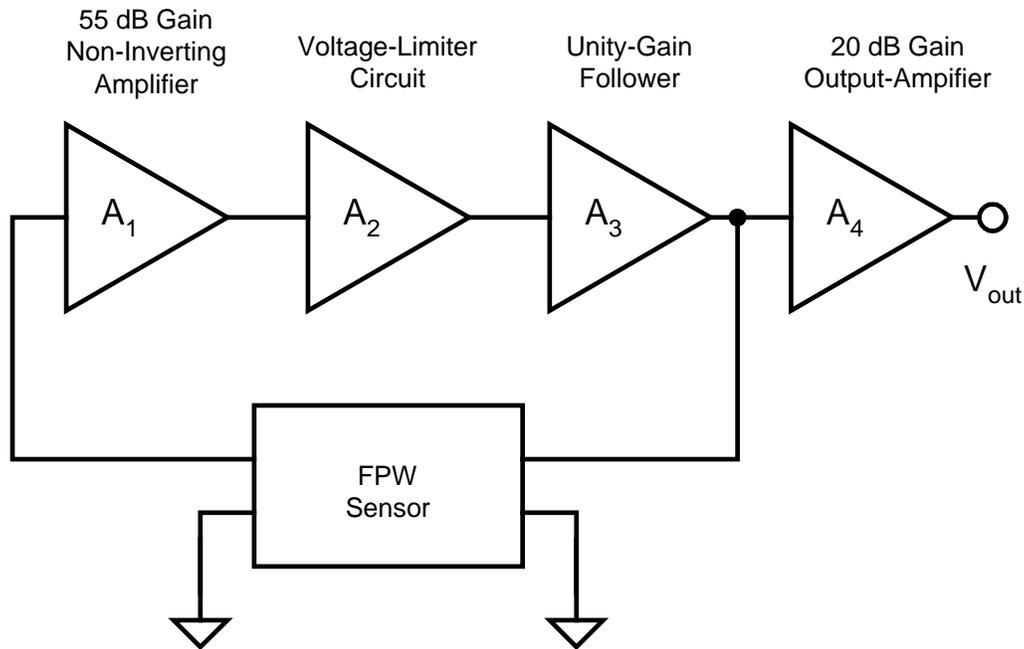


Figure 38. The FPW oscillator block diagram.

$A_1$  is a single high-gain non-inverting amplifier and is the most critical part of the design. The relatively high loss (45 dB at  $0^\circ$  phase) of the FPW requires a high gain amplifier with low phase-shift. In and of itself this is not a large problem considering that the frequency of operation of the FPW is 500 kHz. To accomplish this at low currents (unity mA for this stage alone) becomes a design problem.  $A_2$  is a voltage limiter circuit that provides an amplitude limited square-wave to the buffer amplifier,  $A_3$ , which drives the FPW.  $A_3$  is a unity gain amplifier that is capable of driving the low impedance ( $15\Omega$ ) FPW sensor. The amplifier  $A_4$  is a 20 dB amplifier that is used to drive the next assembly electronics. The signal level at the output of  $A_3$  is a relatively small (100 mV p-p) square wave that is incapable of driving most counter-circuitry, thus  $A_4$  provides a useful signal level for the counter interface electronics of the next assembly.

Simplified schematics for each of the four blocks described above will be shown and discussed individually starting with the high-gain stage  $A_1$ . Figure 39 is a simplified schematic of the high-gain low phase-shift amplifier used in this design.  $Q_1$  and  $Q_2$  are the gain elements of the differential amplifier where  $Q_3$  and  $Q_4$  are an active-load which provides a large gain

$(V_{out}/V_{in})$  while minimizing any Miller effect on the input impedance at the base of  $Q_1$ . Equation 5 describes the gain,  $A_v$  of this amplifier where  $A_v=V_{out}/V_{in}$ .

$$A_v \cong Z_c / ((V_T / I_1) + R_e) \quad (5)$$

$V_T$  is equal to 26 mV at 25° C and  $R_e$  is the bulk emitter resistance ( $Q_1$  and  $Q_2$ ) equal to approximately 10 ohms.

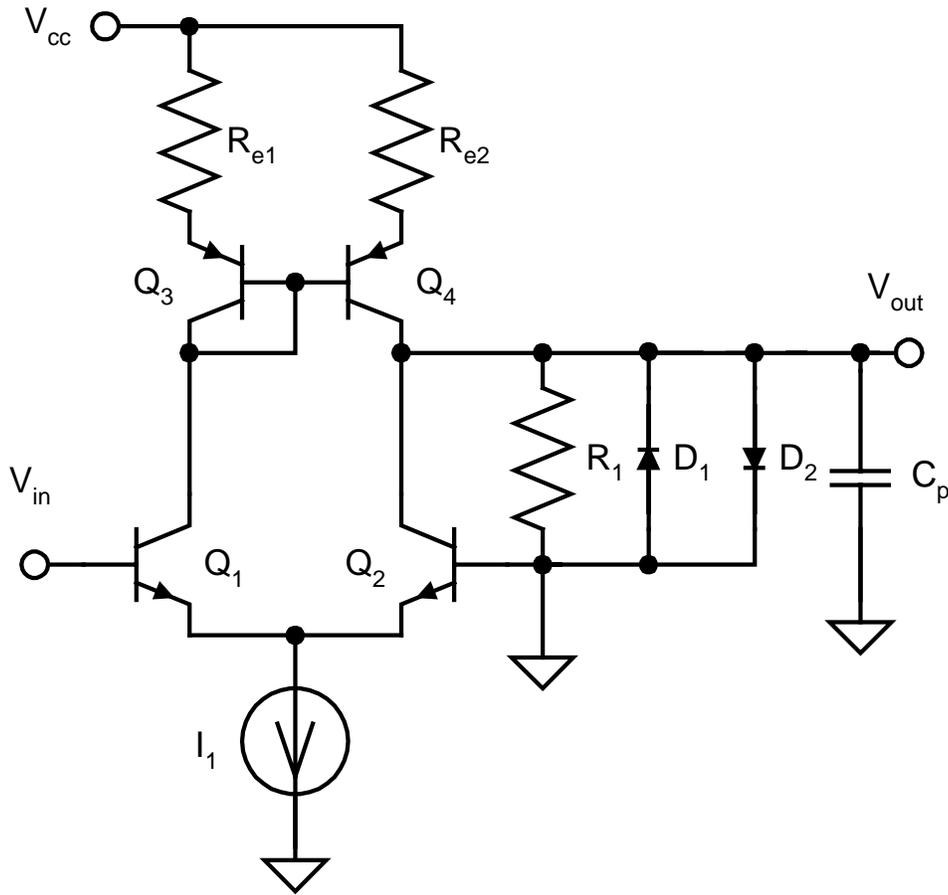


Figure 39. Simplified schematic of circuit block  $A_1$ .

For this circuit  $Z_c$  is equal to  $R_1$  in parallel with the reactance of  $C_p$  in parallel with the output impedance of the differential amplifier. Diodes  $D_1$  and  $D_2$  are used to limit the amplitude of the collector voltage swing ( $Q_2$ ) to approximately 1.4 V peak to peak. This helps maintain a symmetrical waveform around ground at the collector of  $Q_2$  and prevents overdriving the input to the next stage. Letting  $R_o$  equal the output impedance of the amplifier,  $R_o$  equals  $4(V_A/I_1)$  where  $V_A (\cong 15 \text{ V})$  is the early voltage of the transistors. For the transistors used in this design  $V_A$  is approximately 15 V.  $I_1$  was set to 2.6 mA with  $R_1$  chosen to be 30 k $\Omega$ . With these values the voltage gain of the amplifier is approximately 650 or 56 dB.  $C_p$  is a combination of transistor and board parasitic capacitance. This capacitance is approximately 5 pF and causes both a gain limiting and phase-shifting of the gain  $A_v$ . To provide high-gain (55 dB) and low phase-shift ( $< 12^\circ$ ) the current  $I_1$  must be set relatively high with  $R_1$  relatively high.  $R_o$  in parallel with  $R_1$  must

be set to an impedance of approximately five times the reactance of  $C_p$  to obtain an amplifier phase shift of  $< 12^\circ$ . For the lowest possible operating power  $C_p$  must be minimized. To achieve sub-pico Farad capacitances for  $C_p$  an analog ASIC would be required. If either the loss of the FPW is decreased or the capacitance  $C_p$  is decreased the amplifier can provide a phase-shift closer to the  $0^\circ$  ideal. For the optimal frequency stability it is best to operate the oscillator at the maximum phase-slope ( $d\theta/df$ ) of the FPW. This occurs at the zero phase point of the FPW S11. It is not crucial to make the gain function perfectly real ( $0^\circ$  phase-shift) since the FPW S11 phase-slope is approximately the same from  $0^\circ$  to  $\pm 20^\circ$  degrees of phase-shift. Operating too far away from the zero phase point will decrease oscillator stability and also require higher gain, therefore power, to oscillate.

Figure 40 is a simplified schematic of the voltage limiter block,  $A_2$  from Figure 38. This circuit acts as a follower circuit until the input is driven large enough to force this circuit into limiting. The output will limit to a value of  $\pm I_1 R_1$ . In this design  $I_1$  is set to 0.13 mA with  $R_1$  equal to  $390 \Omega$ . This provides a limiting voltage of  $\pm 50$  mV, or 100 mV peak to peak.

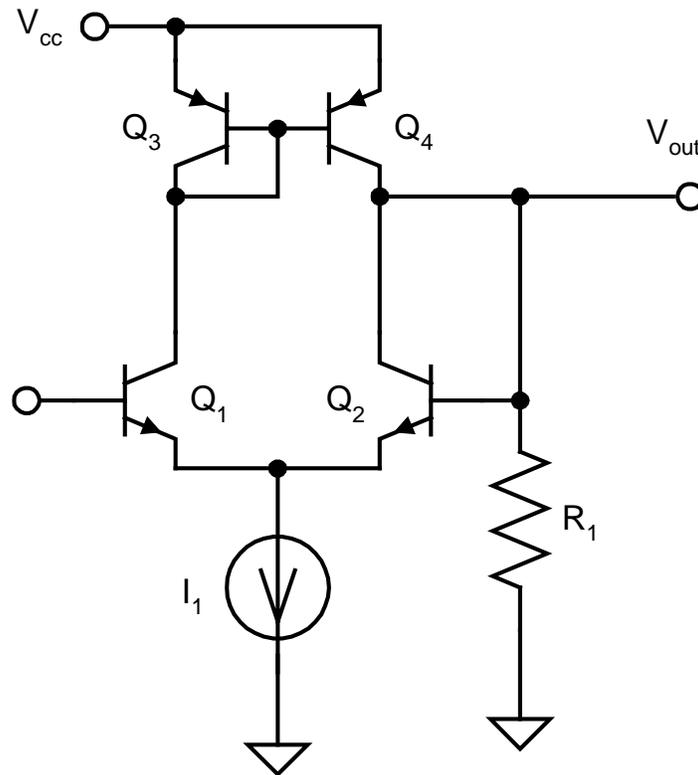


Figure 40. Voltage limiting unity-gain amplifier.

This limiting amplifier has an output impedance equal to  $R_1$ . Since the FPW input impedance is significantly less than this value, the limiter cannot be connected directly to the FPW device and maintain the desired function. A unity-gain buffer circuit,  $A_3$  in Figure 38, provides the necessary buffering. Figure 41 is a simplified schematic of this buffer circuit.  $Q_1$  through  $Q_4$  is a standard differential amplifier configuration.  $Q_5$  through  $Q_8$  comprise a class-B follower circuit that buffers the low-current differential amplifier. The output of the class-B

buffer is feedback to the differential amplifier (base of  $Q_2$ ) which creates a high-performance follower circuit. This design has low offset currents and voltages and provides a very low ( $< 1\Omega$ ) output impedance. This function can be operated at low power due to the high efficiency provided by class-B operation of  $Q_5$ - $Q_8$ .

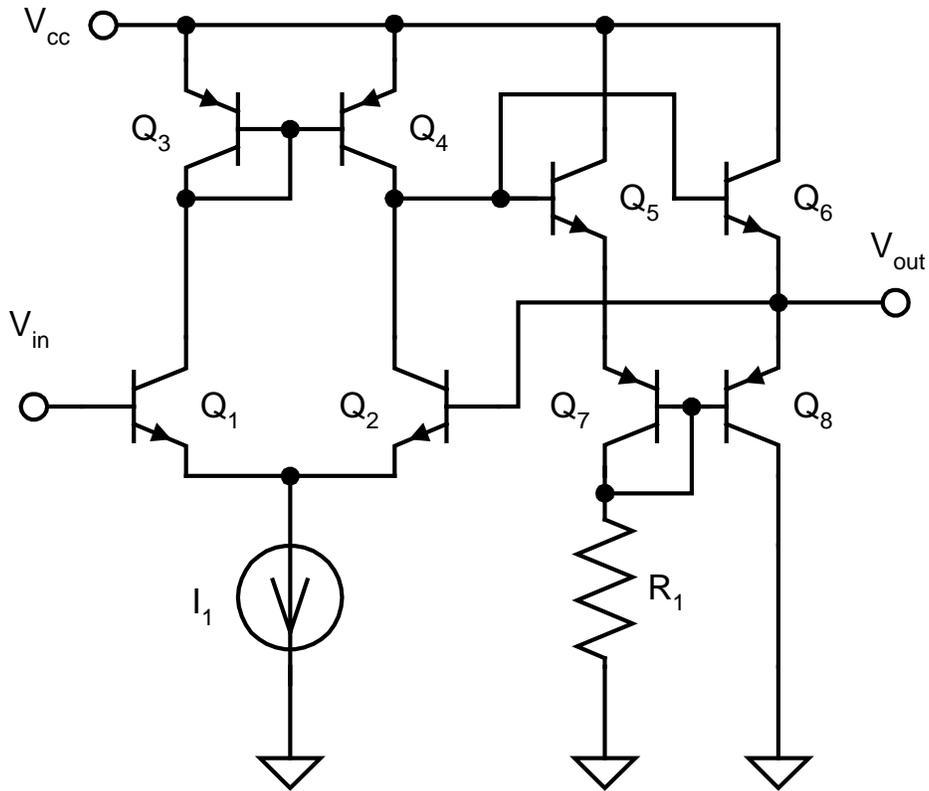


Figure 41. The unity-gain follower circuit.

The value of  $R_1$  sets the bias current of the output stage.  $R_1$  is  $5\text{ k}\Omega$  and sets the idle current of the output transistors to approximately  $600\text{ }\mu\text{A}$ . This current ( $600\text{ }\mu\text{A}$ ) is mirrored in  $Q_5$  and  $Q_7$ . The current source  $I_1$  was set to approximately  $250\text{ }\mu\text{A}$ . Thus the total current for this stage is approximately  $1.5\text{ mA}$ .

The final stage of the oscillator circuit is a  $20\text{ dB}$  gain output-amplifier used to drive the electronics of the next assembly. This amplifier has two internal stages: a gain stage and a class-B driver stage that is identical to the circuit described in Figure 41. Figure 42 is a simplified schematic of the amplifier block  $A_4$  from Figure 38.

The differential amplifier  $Q_1$ - $Q_4$  is a feedback controlled inverting amplifier. Feedback resistors  $R_1$  and  $R_2$  set the amplifier gain. This gain is equal to the ratio  $R_2$  to  $R_1$ . For this application the gain was set to  $10$  ( $20\text{ dB}$ ). Transistors  $Q_5$ - $Q_{12}$  is a unity-gain buffer amplifier that is the same as the circuit described for Figure 41. The complete amplifier circuit raises the  $100\text{ mV}$  peak to peak signal driving the FPW up to approximately one-volt peak to peak. This signal is used to drive the next assembly, which consists of counter circuitry. This circuit uses a total of  $2.4\text{ mA}$ .

The total FPW oscillator circuit, A<sub>1</sub>-A<sub>4</sub> plus the bias circuitry, not described here, draws approximately 10 mA. The total power supply voltage is 10 V, ( $\pm 5$ ) therefore this circuit consumes 100 mW. This current could be brought down significantly if the FPW loss is decreased and/or the parasitic circuit capacitance ( $C_p$ ) is decreased. It would be possible to make such a design operate at 5 to 6 mA given careful design and control of the circuit parasitics.

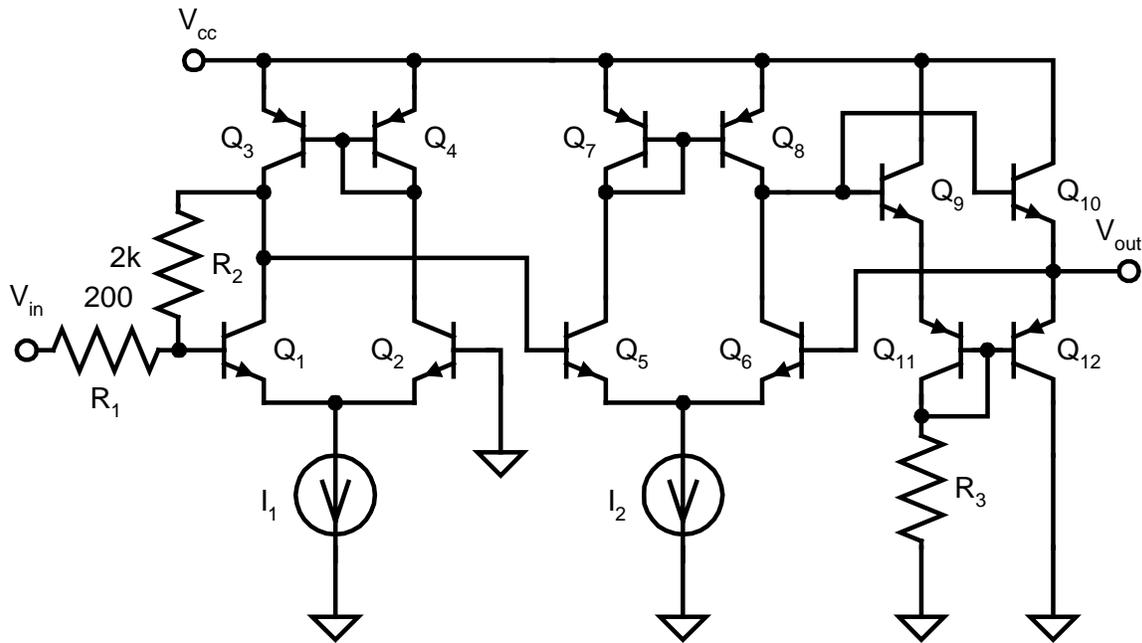


Figure 42. Schematic of the output amplifier of the FPW oscillator.

An FPW ASIC has been developed between 1732 and 1736 using a commercial BiCMOS process. The BiCMOS allows the use of bipolar and MOS transistors on the same die. This allows the design to exploit the high-transconductance of the bipolar transistors in the high-gain stage. The FPW ASIC will be delivered to Sandia in 2/2001.

## CHEMICAL SENSOR DEVELOPMENT

### *SAW Chemical Sensors*

Chemical sensor systems incorporating high frequency surface acoustic wave (SAW) chemical sensors are being developed. The ultimate goal of this effort is a single chip system with the sensor array, drive electronics, and readout electronics monolithically integrated on a GaAs substrate. This device will operate in a DC in/DC out mode with all high frequency circuitry contained on the chip. A schematic of the IC layout and the integrated die, without the SAW sensors, is shown in Figure 43.

As an interim step in this project, a hybrid version of the sensor system has been developed (see Figure 44). In this version, the SAW sensor array has been fabricated on a quartz substrate. The quartz substrate also serves as the printed wiring board to which GaAs ICs containing the RF drive and sense circuitry are attached. Wire bonding provides the electrical interconnection between the ICs and the quartz substrate. Since all high frequency components are contained within the quartz substrate, this device operates in the DC in/DC out mode. The hybrid SAW chemical microsensor array has successfully demonstrated detection of volatile organic compounds, semi-volatile simulants of chemical warfare (CW) agents, and CW agents themselves (Figure 45). Device sensitivity, discrimination, and measurement repeatability are sufficiently good to distinguish between interferants and the CW agents during numerous tests.

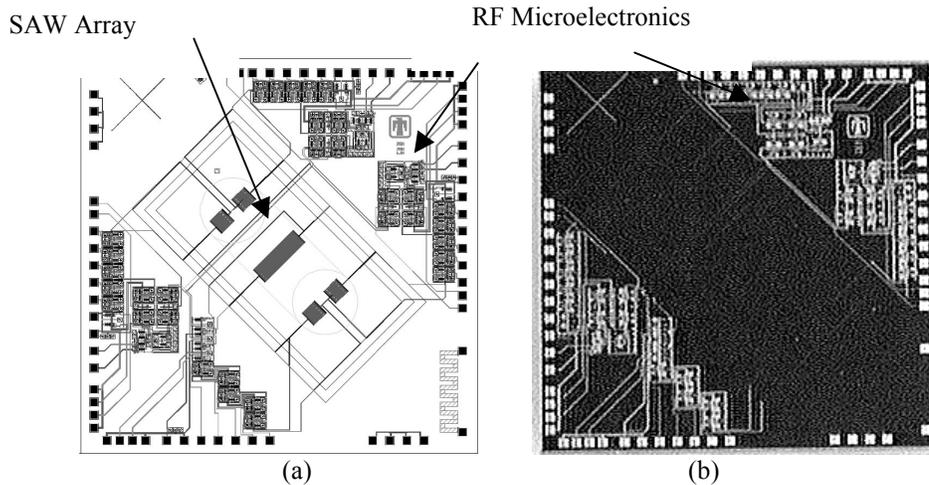


Figure 43. Monolithic SAW Chemical Sensor System. (a) Schematic layout of die showing drive and sense RF circuitry and SAW sensor array. (b) Photograph of IC prior to post-processing in the CSRL to add SAW array. Die size is 4.6 mm by 4.6 mm.

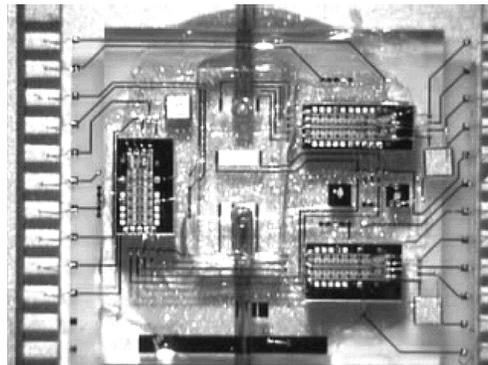


Figure 44. Hybrid Quartz Chemical Sensor System. Quartz substrate has SAW sensors and electrical interconnects patterned directly onto its surface. GaAs ICs provide RF circuitry for DC in/DC out operation. Substrate size is approximately 1 cm<sup>2</sup>.

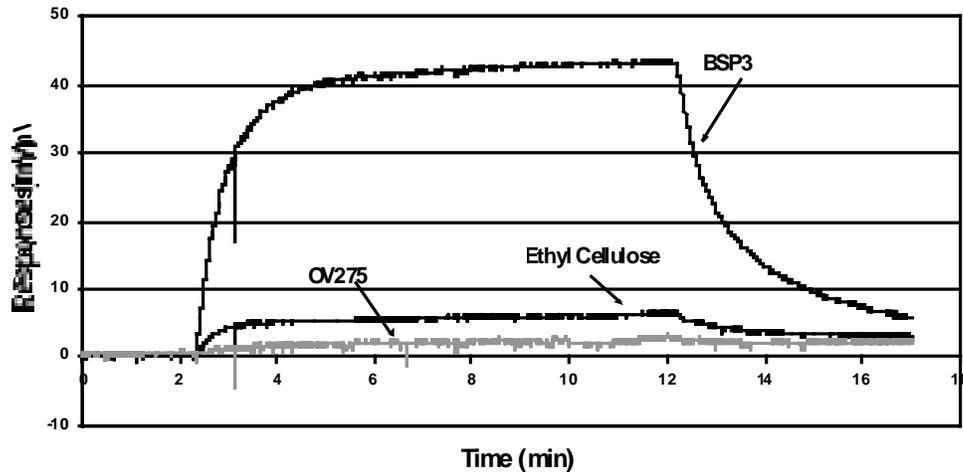


Figure 45. Response of a three-element hybrid SAW array to 15 ppm DMMP. Each element of the array is coated with a different chemically selective polymer layer.

The post-processed integrated GaAs SAW arrays have successfully completed electrical and chemical testing. Post-processed and packaged arrays are shown in Figure 46. Three important goals have been achieved in this area.

1. High sensitivity chemical detection has been demonstrated (Figure 47) with a device that integrates an array of microsensors with the microelectronics required to operate it.
2. Post-processing of commercially fabricated ICs has produced a monolithic device with heterogeneous functions: RF signal processing and chemical sensing.
3. An integrated RF microsystem driven by a monolithic RF oscillator (Figure 48) has been demonstrated.

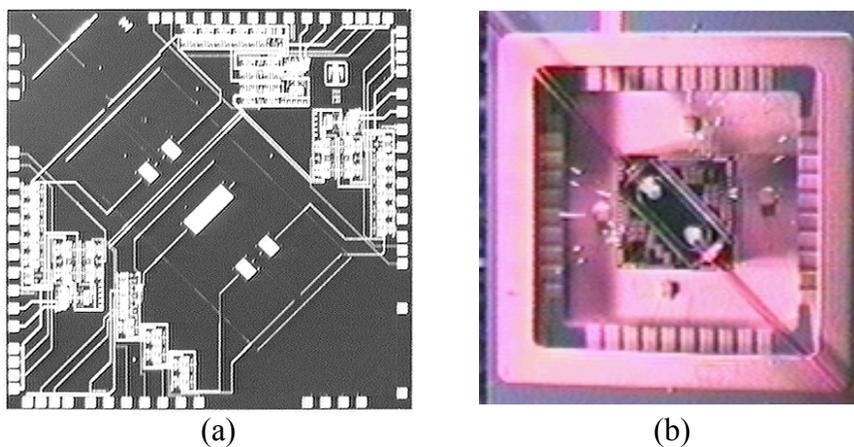


Figure 46. Post-processed, monolithically integrated SAW chemical microsensor array. The SAW sensors and the microelectronics operate at 500 MHz but all chip I/O is DC. This device draws approximately 100 mA at 3 V<sub>dc</sub>. (a) Completed device. (b) Packaged device.

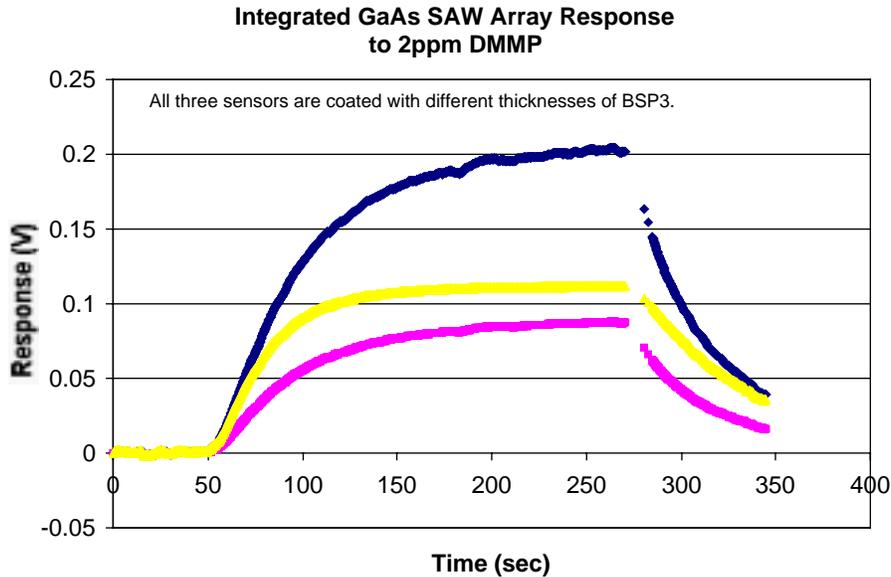


Figure 47. Three-element SAW sensor array response to dimethyl methyl phosphonate (DMMP), a nerve agent simulant, demonstrating sub-part-per-million sensitivity.

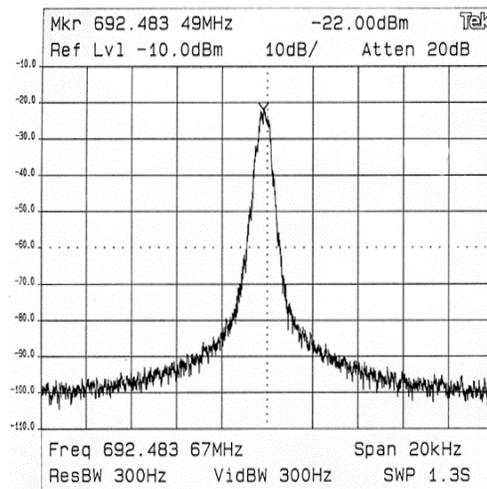


Figure 48. Frequency response of the integrated RF oscillator incorporated in the SAW array. This particular device operates at 700 MHz.

More details of the SAW chemical sensor are included in Appendix B “*Monolithic Integration of GaAs SAW Chemical Microsensor Arrays and Detection Electronics*”.

#### *Chemiresistors*

Relative to SAW chemical sensors, chemiresistors are simple, robust chemical sensors that require only a measurement of DC electrical resistance for readout. A chemiresistor ASIC micro-system has been developed that will “measure” the chemiresistor elements post-processed onto the IC substrate (see Figure 49). The ASIC will accommodate four separate chemiresistors

making a viable array capable of distinguishing a wide variety of chemical species. The electronics are thermally compensated to correct for resistance changes due to temperature variation and include calibration of each sensor via off-chip select components. The ASIC also incorporates high gain for sensitivity and wide dynamic range. The chemiresistor micro-system is designed to measure gas concentrations in the 100's of ppm and higher. A prototype circuit comprised of discrete components on a circuit board was designed and successfully tested. The ASIC can be diced into single-sensor systems for sensor applications that require minimum possible size and only one measurement.

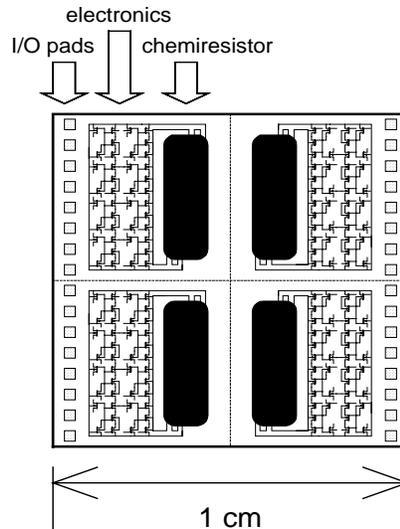


Figure 49. Schematic diagram of chemiresistor ASIC micro-system 4 four separate chemiresistors.

Functional chemiresistor ASICs were produced by post-processing commercially fabricated ICs in Sandia's CSRL to add the chemiresistor sensor (Figure 50). Chemical detection was demonstrated as well as temperature compensation. Some design issues were identified and a second iteration of the chemiresistor ASIC was scheduled for FY2000. Due to a lack of resources in 1736 this goal was not achieved. However, the ASIC has been fully evaluated and design changes and performance goals for the next iteration have been defined. A prototype microrobot that incorporates the chemiresistor ASIC has been assembled (Figure 51). More details of the post-processed chemiresistor ASIC can be found in Appendix C "*Integrated Chemiresistor Array for Small Sensor Platforms*".

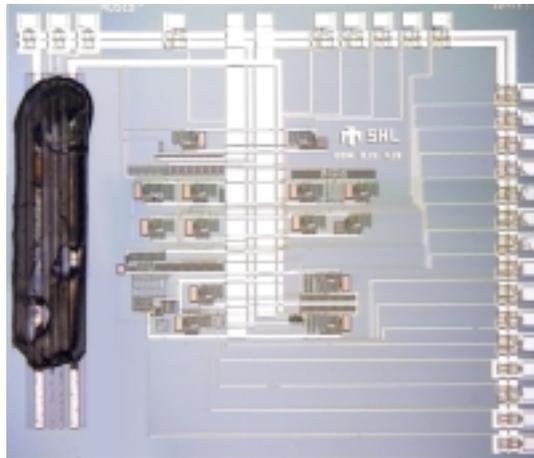


Figure 50. Post-processed chemiresistor ASIC. Chemiresistor sensor is the dark stripe along the left side of the device.

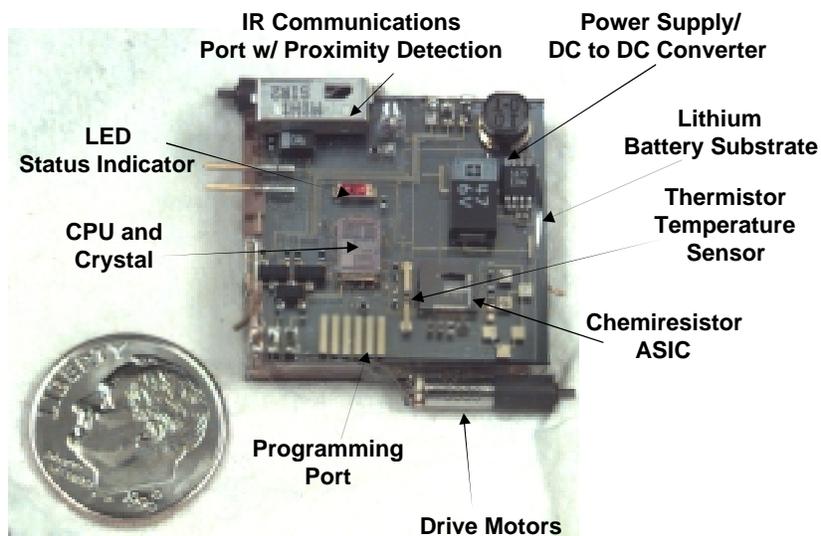


Figure 51. Prototype microrobot with chemiresistor ASIC.

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## **SURFACE MICROMACHINE MICROFLUIDICS: DESIGN, FABRICATION, PACKAGING, AND CHARACTERIZATION**

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### **ABSTRACT**

The field of microfluidics is undergoing rapid growth in terms of new device and system development. Among the many methods of fabricating microfluidic devices and systems, surface micromachining is relatively underrepresented due to; difficulties in the introduction of fluids into the very small channels produced, packaging problems, and difficulties in device and system characterization. The potential advantages of using surface micromachining include: compatibility with the existing integrated circuit tool set, integration of electronic sensing and actuation with microfluidics, and fluid volume minimization. In order to explore these potential advantages we have developed first generation surface micromachined microfluidic devices (channels) using an adapted pressure sensor fabrication process to produce silicon nitride channels, and the SUMMiT process to produce polysilicon channels. The channels were characterized by leak testing and flow rate vs. pressure measurements. The fabrication processes used and results of these tests are reported in this paper.

### **INTRODUCTION**

The field of microfluidics is experiencing rapid growth in terms of both basic research and device development. A variety of microfluidic devices are being developed for applications ranging from  $\mu$ TAS (Micro-Total (chemical) Analysis Systems, Harrison 1998), to ink jet printing (Kamisuki

1998). These devices are fabricated using a wide range of technologies including: bulk micromachining (e.g. KOH etch), high aspect ratio micromachining (e.g. DRIE or LIGA), laser machining, very small scale conventional machining (drilling and milling), capillary tubing assembly and various unconventional techniques (Whitesides 1997). Conspicuously absent from this list is surface micromachining.

Consider as a representative sample the microfluidic papers presented at the ASME winter annual meeting last October (Forster et. al. 1998). Of the 39 papers dealing with experimental microfluidic devices only 3 utilized surface micromachining. Of these 3 papers one (Tseng 1998) was a hybrid design utilizing both bulk and surface micromachining with the flow channels fabricated utilizing bulk micromachining. The 2nd paper utilized surface micromachining to produce valves that controlled flow in much larger passages (Wroblewski 1998). Only the 3<sup>rd</sup> paper (Rasmussen 1998) described flow channels fabricated using surface micromachining. Therefore only 1/39 or 2.6% of the microfluidic papers presented (Forster et. al. 1998) dealt with a microfluidic system in which the primary flow channels were fabricated using surface micromachining.

Despite this lack of utilization, surface micromachining has significant potential advantages over other fabrication techniques in some microfluidic applications. One advantage is volume minimization. A typical bulk micromachined microfluidic device has

a channel depth on the order of  $100\ \mu\text{m}$  and a volume on the order of  $100\ \text{nl}$  (assuming an approximately  $500\ \mu\text{m}$  wide by  $1\ \text{mm}$  long channel). A typical surface micromachined channel is only 2 to  $5\ \mu\text{m}$  deep,  $200\ \mu\text{m}$  wide and  $1\ \text{mm}$  long for a volume on the order of  $1\ \text{nl}$  (2 orders of magnitude smaller). In applications where volume minimization is important (such as  $\mu\text{TAS}$ ) this 2 order of magnitude difference could be significant in reducing mixing times and reagent requirements.

Surface micromachined MEMS devices have been developed with sophisticated electrostatic actuation systems for use in a wide variety of devices ranging from microengines (Garcia 1995) to accelerometers and gyros (Allen 1998). CMOS electronics and MEMS have been integrated on a single silicon substrate in an IMEMS (integrated MEMS) process (Smith 1995). In a similar manner surface micromachined microfluidics can potentially be integrated with electronics to produce electro-microfluidic devices. The additional integration of microfluidics onto a single silicon substrate containing MEMS and/or electronics can lead to a new class of devices, electro-microfluidic MEMS systems on a chip. This class of devices has the potential to accomplish a wide variety of functions (e.g. power generation,  $\mu\text{TAS}$ , hydraulic actuation and control) in a very compact package.

Perhaps the most important reason to develop surface micromachined microfluidics has to do with the tool set used in their manufacture (Smith 1998). This tool set is highly developed for use in IC manufacturing. For this reason it should be relatively easy to go from prototype to mass production with a surface micromachined microfluidic device. In principle such devices can be batch manufactured as inexpensively as electronic integrated circuits.

Before any of these advantages can be realized the packaging challenge must be met. Due to the very small channels produced by surface micromachining ( $<5\ \mu\text{m}$ ), it is very difficult to get fluid into the channels and seal the interface. There is presently no standard method for packaging surface microfluidic devices.

In addition, the performance of surface micromachined microfluidic devices has typically not been completely characterized. In order to use these devices as part of a larger system on a chip or to interface microfluidic devices on a chip with devices external to the chip, the performance characteristics of the microfluidic devices must be quantified. The simplest microfluidic device is a microfluidic channel. Therefore we will focus on the design, fabrication and characterization of very simple microfluidic devices, surface micromachined flow channels. For such simple devices performance is characterized primarily by flow resistance. In this paper, we will attempt to

characterize surface micromachined microfluidic channels in terms of flow resistance.

## DESIGN AND FABRICATION

For surface micromachining in general, surface micromachined MEMS, and surface micromachined microfluidics, device design and fabrication are intimately linked. Device design is constrained by the fabrication process used. In this research two processes were applied to produce two different types of microfluidic channels. Type I channels were fabricated in silicon nitride and were produced using a process developed to manufacture pressure transducers (Eaton 1997). Type II channels were fabricated in polysilicon using SUMMiT ([www.mdl.sandia.gov/Micromachine](http://www.mdl.sandia.gov/Micromachine)). The process flow for type I channels is shown in Fig. 1 (Eaton 1997).

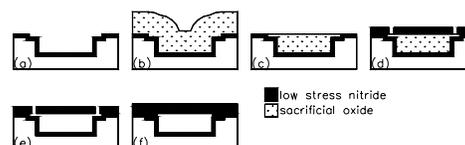


Figure 1. Process Flow for Type I Channels (Silicon Nitride). The fabrication process begins with a trench etched in a silicon wafer and lined with low stress silicon nitride (nitride) (a). The trench is filled with silicon dioxide (oxide) (b). The oxide is polished so that it is even with the top of the nitride using CMP (Chemical-Mechanical Polishing) (c). A thicker layer of nitride is deposited and patterned with etch release holes (d). The sacrificial oxide is removed in an HF (Hydrofluoric acid) release etch (e). The etch release holes are filled during the final nitride deposition (f).

The process begins with a  $2\ \mu\text{m}$  trench etch in a silicon wafer. The trenches are defined using a patterned TEOS (thermal oxide) hard mask. After etching the trenches the TEOS mask is stripped in HF (Hydrofluoric acid) and a  $0.3\ \mu\text{m}$  thick layer of low stress silicon nitride (nitride) is deposited using Low Pressure Chemical Vapor Deposition (LPCVD). After a sacrificial oxide refill the trenches are chemical-mechanically polished (CMP) flat. A  $0.8\ \mu\text{m}$  thick low stress nitride membrane (channel cover) is then deposited over the oxide. The membrane is patterned with etch release holes using another TEOS hard mask, and the release holes are etched using a dry etch. After stripping the hard mask, the structures are released in a 1:1 HF:HCl (Hydrofluoric:Hydrochloric) acid bath. The solution is highly selective – etching the oxide while leaving the nitride alone. Finally the etch release holes are sealed using another LPCVD nitride deposition. The resulting channels are

approximately 2  $\mu\text{m}$  deep. The channels are 200  $\mu\text{m}$  wide at the inlet and outlet and neck down to various widths in between. Fig. 2 is a photograph of a channel and Fig. 3 is a SEM (scanning electron micrograph) image of a channel cross-section.

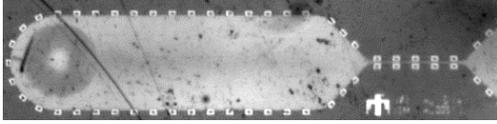


Figure 2. Photograph of Type I channel. The etch release holes are spaced around the channel edge. The channel necks down to 10  $\mu\text{m}$  in width at the left and is 200  $\mu\text{m}$  wide where the Bosch etch hole intersects the channel at the right.

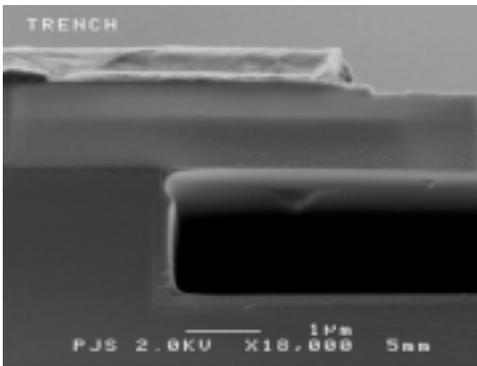


Figure 3. SEM (Scanning Electron Micrograph) of type I channel. The vertical walled channel is slightly less than 2  $\mu\text{m}$  deep, and the bottom and sides are lined with 0.3  $\mu\text{m}$  thick nitride. The top is a 1  $\mu\text{m}$  thick nitride membrane.

In order to introduce fluid at the channel inlet and outlet, via were etched through the wafers from the back using a Bosch process (Bosch 1996). The Bosch process is a Deep Reactive Ion Etch (DRIE) that relies on an iterative deposition/etch cycle in which a polymer etch inhibitor is conformally deposited over the wafer during deposition cycles. The polymer is preferential removed from the bottom of the via due to acceleration of ions perpendicular to the surface of the wafer. Therefore the sides of the via are protected and a vertical walled via results. The Bosch etch via extended all the way through the wafer and were stopped by the nitride layer on the bottom of the type I channels. These via were 200  $\mu\text{m}$  in diameter. Finally the nitride membrane on the bottom of the channel were removed using either a longer exposure to the Bosch process or a Plasma-Therm parallel plate RIE system.

The process flow for type II channels is shown in Fig. 4. A two-level channel is shown. The first level is in the first structural layer of polysilicon (POLY1) and

the second level (top channel cover) is in the 3<sup>rd</sup> structural layer of polysilicon (POLY3). The 2<sup>nd</sup> layer of structural polysilicon (POLY2) is used to fabricate a channel for acid flow during release. Sacrificial oxide layers define the depth of the channels (SACOX1 and SACOX3). Another oxide layer (SACOX2) defines the acid flow channel. During the release process the thin layer of SACOX2 allows acid to flow inside the channels and remove the sacrificial oxide (Silicon Dioxide). Not shown in Fig. 4 is a passage that is defined in POLY2 that allows the acid to attack the oxide between POLY1 and POLY3. Details of the SUMMiT process can be found on the web ([www.mdl.sandia.gov/Micromachine](http://www.mdl.sandia.gov/Micromachine)).

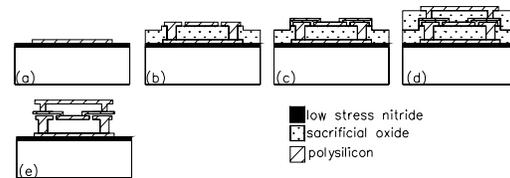


Figure 4. Process Flow for Type II channels (polysilicon). The process begins with deposition of low stress nitride and the bottom layer of polysilicon (POLY0) (a). The first layer of sacrificial oxide (SACOX1) is then deposited, patterned and etched to produce an anchor for the second layer of polysilicon (POLY1) (b). POLY1 is then deposited patterned and etched to produce a channel cover with etch release holes (b). A second layer of oxide (SACOX2) is deposited, patterned and etched (c). A 3<sup>rd</sup> polysilicon layer (POLY2) is deposited over SACOX2 and anchored to POLY1 (c). Another layer of oxide (SACOX3) is deposited and etched for anchoring the 4<sup>th</sup> level of poly (POLY3) (d). POLY3 is deposited to form the top cover of the channel (d). Finally the structure is released by etching away the sacrificial oxide in an HF:HCl bath (e). The channels will be sealed with a sputter deposition of silicon dioxide.

Several different versions of the type II channels in addition to the two level channel shown in Fig. 4 were designed. All of the other designs consisted of one level channels: one design with a POLY1 cover, one with a POLY2 cover, one with a POLY1/2 laminated cover and one with a POLY3 cover. This will result in channel depths of approximately 1.5, 2.0, and 4.5 microns for the various channels.

Type II channels were also Bosch etched from the back side at the channel inlet and outlet to allow fluid to enter and exit. In the SUMMiT process the bottom layer of nitride was removed at the channel inlet and exit using a cut in the nitride layer. Therefore the Bosch etch is stopped on the first layer of oxide (SACOX1) rather than the nitride. During etch release

the channel is hollowed out and the Bosch etch hole from the back is uncovered allowing fluid to enter the channels.

## PACKAGING

Packaging of microfluidic systems is particularly challenging because of the very small size of the fluid channels and sealing requirements. In addition, for these devices we wanted to make the package separate from the surface micromachined microfluidic parts in order to allow different microfluidic devices to be tested with the same packaging setup. Therefore this packaging arrangement is a test fixture for microfluidic devices rather than a production package for inclusion in a larger system.

Both type I and type II channels were fabricated on approximately 5 mm by 5 mm silicon die. They each contained approximately 16 inlet and outlet connections corresponding to approximately 8 channels per die. Each die contains multiple fluid connections, therefore a flow manifold rather than individual microfluidic connectors was utilized. The flow manifold was fabricated from aluminum. The packaging arrangement utilizing the flow manifold is shown in Fig. 5.

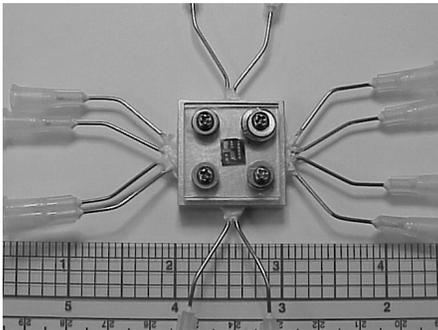


Figure 5. Packaging Arrangement. The 5 mm by 5 mm microfluidic die is shown in the center of the photograph mounted onto the 1 in by 1 in aluminum manifold. The die is held in place by means of a clamping plexiglass plate. The syringe needles allow connection of external fluid lines.

The aluminum flow manifold contains very small drilled holes in the same pattern as the Bosch etch holes in the silicon wafer. These holes intersect larger perpendicular holes drilled from the sides of the manifold. These larger holes are sized to provide a tight fit for 20 gage syringe needles which are epoxied into the holes for sealing. The syringe needle fittings then provide a relatively convenient method for attaching external fluid lines to the manifold.

The holes in the manifold that align with the Bosch holes are 200  $\mu\text{m}$  in diameter and approximately 1 mm apart. A counterbore in the aluminum manifold allows 200  $\mu\text{m}$  inner diameter O-rings (Apple Rubber Products, Lancaster NY) to be placed around these manifold holes. The silicon die is then aligned with the O-ring surrounded holes and clamped down using a plexiglass plate with clamping screws into the manifold. The O-rings compress – sealing the joint between the manifold and the die around each separate fluidic connection. This arrangement allows separate fluids to be plumbed to each microfluidic device on the chip. The resulting sandwich of aluminum manifold, silicon die, and plexiglass cover is leak tight.

The alignment between the manifold and the silicon die is accomplished optically using a low power microscope. The die is placed on top of the manifold with the O-rings in place. A light shines from below through alignment holes in the manifold. These alignment holes line up with corresponding alignment holes in the die allowing precise optical alignment ( $\pm 10 \mu\text{m}$ ). The 3.175 mm thick plexiglass plate is then placed over the die and tightened to the manifold using 4 screws to complete the assembly.

## DEVICE CHARACTERIZATION

As microfluidics moves out of the laboratory and into industrial, commercial and military application device reliability and performance become more and more important. Almost all microfluidic devices at the simplest level are concerned with flow through very small flow passages. Therefore one reasonable way of characterizing microfluidic devices is in terms of their flow rate and the pressure required to achieve that flow rate. For electrically powered flows it makes more sense to measure flow rate as a function of voltage, current or power. However in either case, the flow resistance of the channels characterizes the severity of viscous effects.

In addition microfluidic systems can be characterized in terms of how leak tight they are. This is particularly the case for gas flow systems. In liquid systems surface tension acts to prevent leaks, and at microfluidic scales surface tension is a significant force. On the other hand the pressures developed even at very low flow rates are significant in microfluidic systems. Therefore microfluidic systems must be leak tight to very high pressures.

For any characterization the entire package must be considered. When checking for leaks, for instance, the characterization is not so much of the surface micromachined microchannels but of the die/package assembly. In addition the characteristics of the measurement system must be considered when evaluating the microfluidic system. For instance when using a syringe pump to develop a

controlled flow rate in a microfluidic channel the large volume of the syringe relative to the microfluidic channel must be considered.

**Package Sealing**

Package sealing was characterized using two techniques; a helium leak test apparatus, and a gas tight syringe pump. The vacuum test apparatus involves pulling a vacuum inside the microfluidic channels and testing for leakage of helium from outside the channels to inside. The gas tight syringe tests involved pressurizing the channels using the syringe pump and checking measured pressure vs. volume characteristics vs. those predicted using the ideal gas law for a sealed container. Deviations from ideal gas law predictions can be related to a leak rate.

In terms of liquid flow, leak rates above the evaporation rate can be determined from observation. Pressures as high as 50 *Atm* were measured with no observable liquid leak. The evaporation rate was measured as approximately 10 *nl/s* by weighing a volume of water with a sensitive scale as it evaporated from an approximately 1.5 *cm* diameter graduated cylinder. The surface area of the water exposed to evaporation was approximately  $1.77 \times 10^{-4} \text{ m}^2$  during the evaporation measurement. The evaporation rate per unit area was therefore approximately  $56 \mu\text{l} / \text{m}^2 \cdot \text{s}$ . The area for evaporation between the O-ring and the manifold was estimated at approximately  $6.3 \times 10^{-10} \text{ m}^2$  (assuming a 1  $\mu\text{m}$  gap around the O-ring outer diameter). Therefore the evaporation rate for the manifold assembly is estimated as 35 *fl / s Atm*. The reason the evaporation rate is so low is that evaporation can only occur in the very small gap between the O-ring and the manifold or silicon wafer interfaces.

**Helium Leak Tests.**

The manifold assembly was leak tested using a vacuum leak test machine (Varian Vacuum Products, Lexington MA). A sealed stainless steel tubing line connected the microfluidic assembly to the leak testing machine. The connecting line was verified as leak tight using the leak testing machine. The line was then attached to one flow channel input line and the connection was sealed. The downstream exit from the channel was sealed at the manifold exit of the channel.

The first step of the leak check process was to evacuate the sealed volume, which includes the microfluidic channel, its inlet and outlet manifold passages, and the connecting tubing. This volume was evacuated to a pressure of < 1 *mTorr*, which is approximately 0.001 % of an atmosphere, using a vacuum pump built into the vacuum tester. Therefore there is a pressure difference of approximately 1 *Atm* between the inside and outside of the sealed volume.

This level of pressure difference is required for the vacuum tester to operate.

A separate helium line is then used to introduce helium around the device. The exit of the helium line was a small needle that was used to place helium precisely at all the joints of the assembly. A mass spectrometer then measured the amount of helium that leaked through the assembly into the connecting tubing to reach the mass spectrometer. Five measurements were taken on three different manifold assemblies. A leak rate of:

$$1.6 \pm 4 \times 10^{-11} \text{ l/s Atm} \tag{1}$$

of helium was measured. This leak rate applies for conditions of approximately 1 *Atm.* of Vacuum in the channel.

**Syringe Pump Leak Tests.**

Leak tests for positive pressure difference (pressure inside the channel higher than atmospheric) were conducted using a gas tight 50 ml syringe (Hamilton Syringe, Reno NV) and a syringe pump (Harvard Apparatus, Cambridge MA) to pressurize air contained in the combined syringe, manifold, channel and connecting tubing volume. The manifold channel exiting the microchannel was sealed providing a closed volume.

The nitride membrane channel covers deflect under the positive pressure (Fig. 6). From the interference fringe pattern shown (3 fringes) a maximum membrane deflection of approximately 0.8  $\mu\text{m}$  was calculated.

$$d = 3 \times \frac{\lambda_{avg}}{2} = 825 \text{ nm} \tag{2}$$

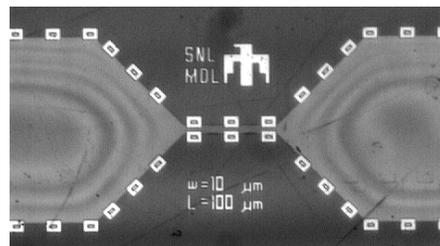


Figure 6. Leak Test Membrane Deflection. Type I channel pressurized to approximately 3.5 *Atm*. Light passing through the channel cover reflects off the bottom of the channel and cancels or enhances light reflected off the channel cover to produce the fringe pattern.

Pressure measurements just upstream of the microchannel manifold were used to calculate the excess mass of air contained in the volume. The excess mass of air is the mass of air in addition to that which would be contained in the volume at

atmospheric pressure. Gauge pressure was measured at an in-line pressure measurement T between the syringe pump and the microfluidic manifold. One leg of the T connected to a very small pressure transducer (Entran Devices Inc., Fairfield NJ) and the other two legs provided the inlet and outlet for the feed through.

As air leaked from the volume the gauge pressure dropped (Fig. 7). Two different microfluidic manifold assemblies were tested. The 4/10/1999 data was taken on a manifold assembly that contained a gasket spacer between the plexiglass cover and the manifold. The 3/12/1999 data manifold assembly did not utilize the spacer. The gasket spacer provided more even clamping of the plexiglass cover plate. The 4/10 data did not show the nitride membrane deflection that the 3/12 data did (Fig. 6), due to this more even clamping.

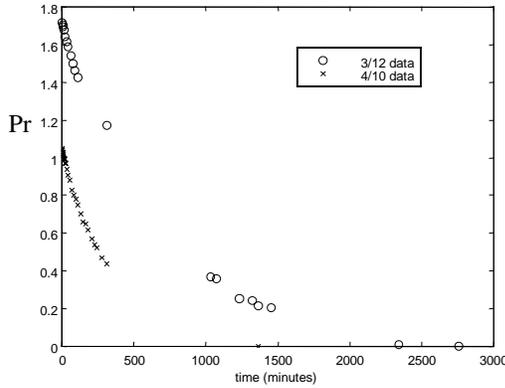


Figure 7. Leak Test Data. Pressure ratio (Pr),  $(P - P_{atm}) / P_{atm}$ , decays as air leaks out of two different microfluidic manifold assemblies.

The exponential decay in pressure was related to the leakage by fitting the curve of mass contained in the volume vs. time. Using the ideal gas law:

$$m_{excess} = \frac{P \cdot V}{R_{air} T}, R_{air} = 286 \frac{J}{kg K}, T = 295.22 K \quad (3)$$

$$V = 28 ml \quad 3/12 \text{ data}, \quad V = 25.5 ml \quad 4/10 \text{ data} \quad (4)$$

$$\begin{aligned} m_{excess} &= 3.316 \times 10^{-10} \times P \quad 3/12 \text{ data}, \\ m_{excess} &= 3.02 \times 10^{-10} \times P \quad 4/10 \text{ data} \end{aligned} \quad (5)$$

The natural log of this calculated excess mass is plotted vs. time in Fig. 8. The inverse of the slope of the resulting straight lines is the time constant for the exponential decay curves.

$$m_{excess}(t) = m_0 \cdot \exp\left[-\frac{1}{\tau} \cdot t\right] \quad (6)$$

Differentiate with respect to time to calculate leakage.

$$\frac{dm_{excess}(t)}{dt} = -m_0 \left[ \frac{1}{\tau} \right] \exp\left[-\frac{1}{\tau} \cdot t\right] \quad (7)$$

Leak rates are typically normalized by pressure to get units of (l/sec-atm)

$$P(t) = P_0 \cdot \exp\left[-\frac{1}{\tau} \cdot t\right] \quad (8)$$

$$\frac{dm_{excess}(t)}{dt \cdot P} = -\frac{m_0 \cdot (1/\tau)}{P_0} \quad (9)$$

Using this relationship calculate the leak rate (LR),

$$\begin{aligned} LR &= 0.445 \frac{\mu l}{s \text{ Atm}} \quad 3/12 \text{ data}, \\ LR &= 0.62 \frac{\mu l}{s \text{ Atm}} \quad 4/10 \text{ data} \end{aligned} \quad (10)$$

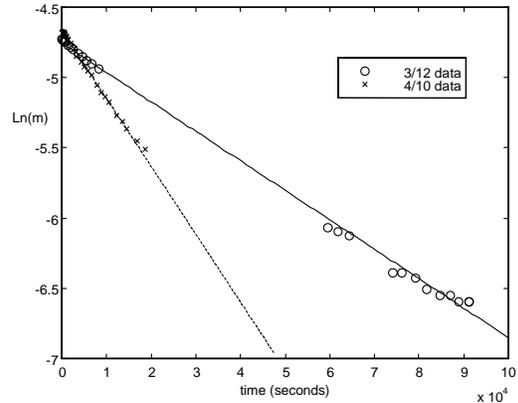


Figure 8. Measured Leak Rates. The slope of the natural log of the excess mass,  $\ln(m)$ , decay curve was used to calculate the leak rate.

Air flow in the channel was investigated by opening the downstream manifold passage. The pressure downstream of the flow constriction was atmospheric (see Fig. 9), while the pressure upstream of the flow constriction remained high – approximately 3.5 Atm.

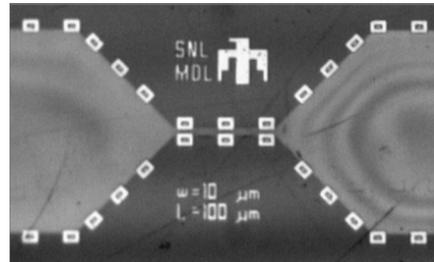


Figure 9. Membrane Deflection – downstream end open. Air flow right to left.

The pressure ratio across the flow constriction was large enough to establish choked flow in the constriction. If we ignore viscous losses:

$$m_{air} = \frac{0.0405 \times P_{upstream}}{\sqrt{T}} \times A_{constriction} = 14 \frac{\mu l}{s} \quad (11)$$

**Liquid Flow.** Three sets of pressure vs. water flow rate data were measured for three different manifold assemblies. When water was pumped into the first channel/manifold assembly using the syringe pump, an air bubble was trapped in the inlet to the channel (see Fig. 10). In larger flow passages (e.g. a 50  $\mu m$  deep channel or a capillary tube) trapped air bubbles assume a characteristic rounded shape at each end. However in these surface micromachined microfluidic channels the air bubbles assumed an irregular shape. As water flowed through the channel a part of the air bubble broke off and squeezed through the channel. These air bubbles followed regions where the channel was deflected inward by low pressure (see Fig. 11). The air bubbles moved very rapidly between these regions. Other bubbles moved through regions that were not deflected inward much more slowly.

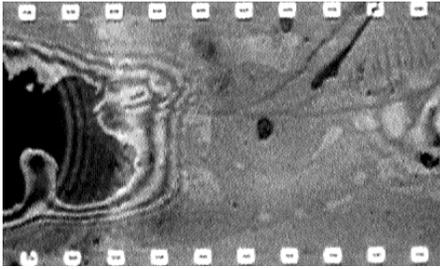


Figure 10. Bubble at Channel Inlet. Water flow from left to right. Channel inlet at far left. The air bubble trapped at the inlet assumes an irregular shape with approximately 3 fringes around it. At the far right a 2<sup>nd</sup> fringed region is beginning.

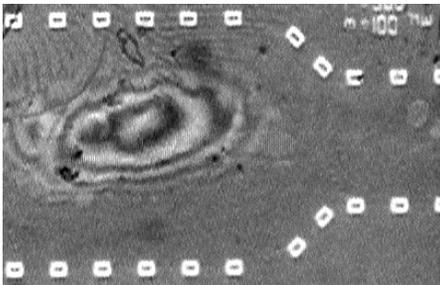


Figure 11 Low Pressure Region Upstream of Flow Constriction. The 2<sup>nd</sup> fringed region is just upstream of the flow constriction. Large air bubbles move very rapidly between the two low pressure regions and then through the constriction.

The 2<sup>nd</sup> and 3<sup>rd</sup> manifold assemblies tested did not have a bubble trapped at the inlet because they were assembled with water already filling the manifold channels. When the silicon wafer was clamped in position this water was drawn into the channels effectively eliminating any possible bubble formation locations at the manifold/wafer interface. These assemblies did not show bubbles anywhere in the channel after a short flush out period. The difference between the 2<sup>nd</sup> and 3<sup>rd</sup> assemblies was the amount of tightening used to attach the clamping plexiglass cover. The 3<sup>rd</sup> (higher slope case – Fig. 12) was significantly tighter and the channel showed significantly higher flow resistance.

The flow resistance for each assembly was calculated from the slopes of Fig. 12 as:

$$1.08 \times 10^{15} \frac{N \cdot s}{m^5}, \quad 1st \text{ assembly} \quad (12)$$

$$4.26 \times 10^{15} \frac{N \cdot s}{m^5}, \quad 2nd \text{ assembly} \quad (13)$$

$$4.15 \times 10^{16} \frac{N \cdot s}{m^5}, \quad 3rd \text{ assembly} \quad (14)$$

The theoretical flow resistance can be calculated from the Poiseuille slot flow equations (White, 1994).

$$R_{flow} = \frac{12 \times \mu}{b^3} = \frac{12 \times 10^{-3}}{(2 \times 10^{-6})^3} = 1.5 \times 10^{15} \frac{N \cdot s}{m^5} \quad (15)$$

The measured flow resistance for the 1<sup>st</sup> and 2<sup>nd</sup> assemblies bracket the theoretical flow resistance. The more tightly clamped 3<sup>rd</sup> assembly had a significantly higher flow resistance. Fringe patterns were observed in the 3<sup>rd</sup> assembly nitride membrane indicating that the plexiglass plate was deforming the silicon nitride channel covers, probably causing the higher flow resistance.

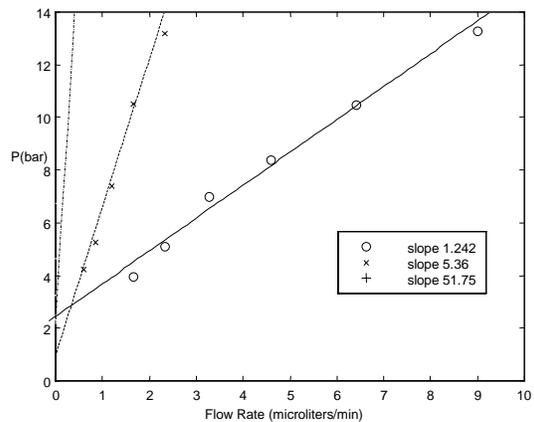


Figure 12. Water Flow Resistance. The slope 1.242 case corresponds to Figs. 10 and 11.

## SUMMARY

The results of this research indicate that the challenges hindering the development of surface micromachined microfluidics can be overcome. We have demonstrated that 1<sup>st</sup> generation surface micromachined microfluidic devices (type I channels) were sealed to leak rates of  $16 \text{ nl} / \text{s Atm}$  for helium at a vacuum,  $0.5 \mu\text{l} / \text{s Atm}$  for air at high pressure, and  $< 35 \text{ fl} / \text{s Atm}$  for water. The flow resistance for type I channels was measured near the predicted flow resistance of  $1.5 \times 10^{-5} \text{ N s} / \text{m}^5$  for water flow. Further testing of both type I and type II channels is planned to quantify the effects of channel width variation on flow resistance, measure flow resistance for air, silicon oil, and methanol flow, and to quantify uncertainties in flow resistance.

Leak rate and flow resistance were sensitive to the microfluidic package assembly process. Both the method and tightness of assembly had a dramatic effect on measured leak rate and flow resistance. Therefore a consistent manifold assembly process must be developed to achieve predictable microfluidic device performance.

In addition to pursuing a more consistent packaging solution we plan to build and characterize more complicated surface micromachined devices that integrate microfluidics and electronic actuation. The integration of microfluidics and electronic actuation will enable a broad range of revolutionary new applications achievable with sacrificial surface micromachining technology.

## ACKNOWLEDGEMENT

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# MONOLITHIC INTEGRATION OF GaAs SAW CHEMICAL MICROSENSOR ARRAYS AND DETECTION ELECTRONICS

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## ABSTRACT

We describe the integration of an array of surface acoustic wave delay line chemical sensors with the associated RF microelectronics such that the resulting device operates in a DC in/DC out mode. The microelectronics design for on-chip RF generation and detection is presented. Both hybrid and monolithic approaches are discussed. This approach improves system performance, simplifies packaging and assembly, and significantly reduces overall system size. The array design can be readily scaled to include a large number of sensors.

## INTRODUCTION

In many of chemical sensing applications, sensor size is a critical system constraint, where smaller size generally translates into lighter weight, smaller sample volumes, lower power consumption, and greater portability. Small sensors are also more readily arrayed into a system with a high degree of chemical discrimination, capable of operation in the complex chemical backgrounds found in real-world environments. However, a reduction in the size of the chemical transducer is not sufficient to reduce the overall sensor system size significantly, since system size is often determined by the control electronics, electrical interconnections, and packaging. To bring about a significant reduction in system size, these other components must be considered as well. For chemical transducers that can be produced on semiconductor substrates, the monolithic integration of the transducer with its control electronics, through the use of integrated circuit (IC) microfabrication technology, can bring about the desired size reduction. Other benefits as well often accrue with monolithic integration, including enhanced manufacturability and reliability, minimized temperature dependence, simplified packaging and assembly, and reduced cost.

Gallium arsenide (GaAs) is an intriguing semiconductor material for the particular case of acoustic wave chemical sensors, when viewed in terms of integration. GaAs is intrinsically piezoelectric, which permits electrical generation of acoustic waves. A mature GaAs IC technology also exists, with commercial foundries able to provide application-specific integrated circuits (ASICs) from a customer's design. Coincidentally, this IC industry has driven two developments critical to integrated acoustic wave sensors: high purity, low defect density, crystalline GaAs substrates suitable for acoustic wave generation and high frequency analog ICs required to generate and detect the acoustic signals. Thus, the foundational technologies required for integrated GaAs acoustic wave chemical sensors are in place.

Acoustic wave chemical sensors operate at high frequencies, typically between 100 MHz and 500 MHz, because chemical sensitivity generally increases with acoustic frequency [1]. This frequency range underscores the importance of monolithic integration for this particular application. In addition to the advantages listed above, a device that contains all high frequency

electronic and acoustic components on a single substrate is expected to have improved performance because of a reduction in losses associated with transferring high frequency signals between discrete components. GaAs is particularly well suited for high frequency microelectronics integration, making complete direct current (DC) -in, DC-out operation on a single chip a realizable goal.

## SURFACE ACOUSTIC WAVE SENSOR DESIGN

As shown in Figure 1, surface acoustic wave (SAW) delay line sensors consist of a piezoelectric substrate and two interdigitated transducers (IDTs) formed by photolithographic patterning of a thin metal layer. Application of an alternating voltage to the input transducer generates an alternating strain field that launches a surface acoustic wave. The acoustic wave travels along the substrate surface before being converted back into an electrical signal by the output transducer. The time delay resulting from the transit of the acoustic wave between the IDTs gives rise to the name of these devices.

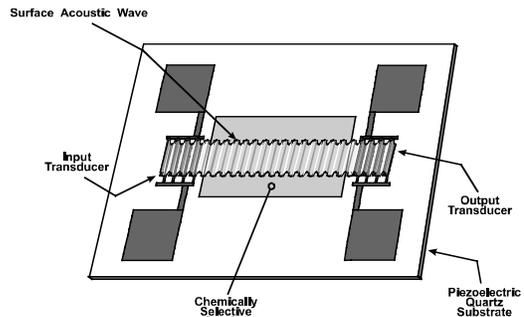


Figure 1. Schematic of a SAW delay line sensor.

The velocity and attenuation of the propagating wave are very sensitive to properties such as mass, temperature, and viscoelasticity of thin films formed on the device surface. For example, increases in surface mass loading decrease the SAW velocity. This property can be used to detect picogram mass changes [1]. By coating the acoustic path with a material that sorbs a chemical species of interest, this sensitivity can be used to develop chemical sensors [1-3]. When configured in an oscillator circuit, as shown in Figure 2, changes in the delay line acoustic velocity,  $\Delta V_R$ , which is equivalent to a phase change,  $\Delta\theta$ , can be observed as a frequency shift,  $\Delta f$ . This oscillator approach converts a very small velocity change into a measurable frequency increment, which can be determined with parts per billion resolution. In the limit of small perturbation, the response to these surface changes can be expressed as:

$$\frac{\Delta f}{f_o} = \frac{\Delta\theta}{\theta_o} = \frac{\Delta V_R}{V_{R_o}} = -k_m \frac{\Delta m}{m_o} - k_T \frac{\Delta T}{T_o}, \quad (1)$$

in which  $m$  is the surface mass,  $T$  is the temperature,  $k_m$  is the mass sensitivity and  $k_T$  is the temperature sensitivity.

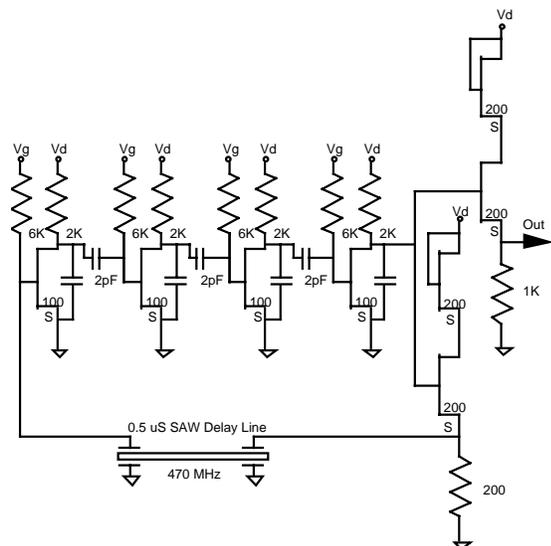


Figure 2. Schematic of a 470 MHz SAW oscillator circuit.

GaAs SAW delay lines are fabricated on (100) semi-insulating substrates with the delay lines oriented in the [011] direction. These substrates are standard for microelectronics applications and the [011] direction maximizes the coupling between electromagnetic and acoustic waves. These delay lines operate between 100 MHz and 500 MHz, where the pitch of the IDT finger pairs determines the frequency of the device. Typically, each IDT contains 50 finger pairs. The input and output IDTs are separated by 190 acoustic wavelengths and are 30 wavelengths wide. IDTs consist of a 500 Å to 1000 Å thick gold layer (depending on device frequency) on top of a 200 Å thick titanium adhesion layer, deposited by thermal evaporation.

### SAW SENSOR ARRAY

Because of the limited selectivity of the sorbing coatings applied to SAW chemical sensors, a single SAW sensor is insufficient to identify analytes in a realistic background of interferants. In practice, an array of sensors, each with a different selective coating, is used to make reliable chemical identification. An array of sensors also allows redundancy and error-checking, important advantages in the overall system. Multiple sensors are also commonly used to compensate for undesired sensor responses. In a classic dual sensor system, two sensors are maintained in identical environments except one is introduced to the desired stimulus. The resulting responses (frequencies) can then be subtracted to allow for removal of the undesired background responses due to temperature or other surface changes.

Figure 3 shows a block diagram of a novel dual-sensor approach that allows for integration and can be scaled to larger array size. In this system, phase is compared (subtracted) rather than frequency. One SAW device (Ch R) is used as a reference channel and is assumed isolated from the surface stimulus of interest. The reference oscillator drives a second acoustic channel (termed test channel, Ch T) on the same substrate. Note the unique use of the acoustic wave propagating in either direction from the center IDT to provide the necessary power split of the reference and test channels. Multiplying the test signal with the reference signal and observing the DC component of the result performs the phase difference. A parasitic second harmonic is present at the phase output and is filtered off. It should be noted that this approach has converted the velocity change into a voltage change.

This allows for easy measurement with low-cost electronics, but also undoubtedly loses resolution compared to a time measurement.

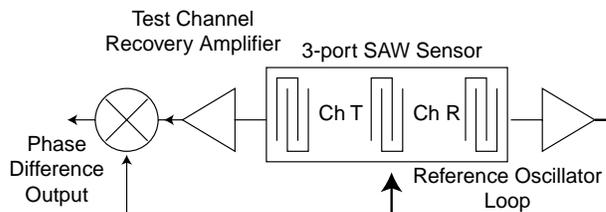


Figure 3. Block diagram of a dual-channel (3-port) SAW sensor system.

This design compensates for changes in the sensor temperature. Since the two acoustic paths are on the same substrate, they can be assumed to be at exactly the same temperature. Therefore, referring back to Equation (1) and assuming that only the test channel experiences the mass uptake, the temperature effects will exactly cancel and only the mass uptake of the test channel will be present at the output. This compensation is almost perfect except for the slight change in mass sensitivity as the reference channel center frequency changes over temperature. Additionally, this approach is tolerant to “mode-hopping” (changes in the longitudinal mode number) due to the subtractive nature of the technique. In practice, the necessary application of the chemically selective thin film to the test channel will change the temperature coefficient of the test channel and compromise the complete elimination of the temperature terms in the subtraction. This unfortunate effect will be an issue for any measurement approach and substrate material.

### SAW ARRAY ELECTRONICS DESIGN

The dual-channel temperature compensated SAW sensor approach is readily extended to large arrays of acoustic sensors. A schematic of a four-element SAW delay line array configuration is shown in Figure 4. A large bi-directional central transmitting IDT spans each of four smaller receiving transducers. Appropriate chemically sorbent coatings are applied to three of the regions between the transmitting IDT and the receiving IDTs, with the fourth left uncoated to provide a reference phase for the array. As in the dual sensor system, an oscillator circuit drives the transmitter, launching an acoustic wave to the receivers. Phase comparator circuitry measures the relative phase of each of the receivers with respect to the reference and provides a DC output voltage proportional to the relative phase. The block diagram of a four-channel system, including electronic circuitry, is shown in Figure 5. Extension to n-channels simply requires splitting the reference signal  $2n-1$  ways (n inputs for each acoustic channel and mixer drive for n-1 channels).

The electronics diagramed in Figure 5 incorporate several novel design features. All signals represented by single lines in this figure are implemented differentially in the actual design. The amplifier blocks shown as triangles are specially designed limiting differential amplifiers providing small phase errors at large overdrive conditions. The amplifiers also provide a log output signal, which allows for an accurate power measurement of the signals from each SAW output port. This permits measurement of the insertion loss of each SAW channel. The mixers are implemented as Gilbert cell mixers, which homodyne the test signal to DC. The input signals to the mixers are hard limited (square waves) by the amplifiers so in effect the mixer operates digitally, performing the

exclusive-or function. This provides linear phase detection and provides two-quadrant phase detection as shown in Figure 6. This detection response provides a unique output if the two signals' phase difference remains within the appropriate two quadrants of phase space (1 and 2 or 3 and 4).

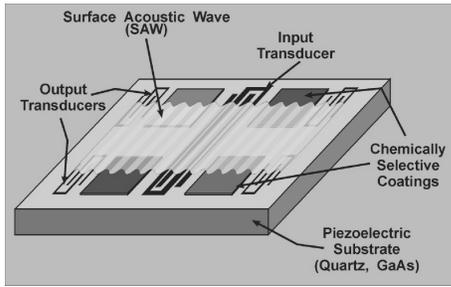


Figure 4. Schematic of an array of four surface acoustic wave devices on a single substrate.

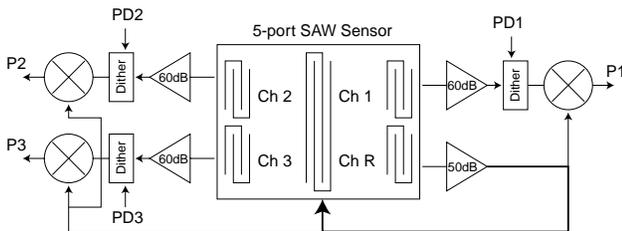


Figure 5. Block diagram of a four-channel (5-port) SAW sensor system.

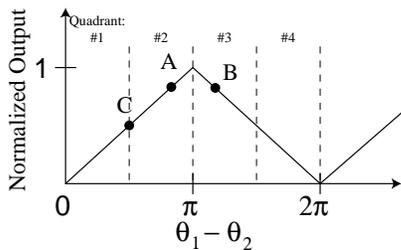


Figure 6. Diagram of the normalized DC component from the Gilbert cell mixer.

To achieve the desired full four-quadrant phase detector, the phase “dither” circuits as shown in the block diagram were added. The phase dither circuits allow for a given test channel to be selectively advanced or retarded in phase by a fixed predetermined amount. Inputs are provided to cycle through three phase states to determine the phase uniquely over the complete  $2\pi$  phase space. Operation of the dither sequence can be illustrated by an example shown by the three labeled points in Figure 6. Assume the actual phase is at the point A. From a single DC output measurement, one cannot determine if the actual phase is in quadrant #2 or quadrant #3 (normalized output is the same at points A and B). Using the phase dither, the response curve can be “shifted” to determine the “slope” of the output and hence the correct quadrant. Assuming that the dither shifts the output from point A to point C, the negative slope indicates the actual point is in quadrant #2. Three dither states are provided to handle the event where the measured and dithered points straddle a quadrant boundary (as with points A and B in Figure 6). In general all three dither states must be considered to guarantee unique phase detection over all phase space.

## HYBRID FOUR-ELEMENT SAW ARRAY

An array of SAW sensors and the associated microelectronics was first produced using a hybrid packaging approach rather than through monolithic integration [4]. Although it requires more assembly than the monolithic approach, the hybrid device prototypes can be produced more rapidly and can be used to test the sensor design and circuit functionality. It also represents a significant size reduction compared to conventional SAW sensor systems.

The SAW array is fabricated on a ST-quartz substrate. In this case, quartz was selected because the requirement for monolithic integration was removed and quartz has slightly better acoustic performance than GaAs. The oscillator amplifier and phase comparator circuitry are custom GaAs ASICs attached directly to the quartz substrate. Metal paths patterned directly onto the quartz die provide circuit interconnection. Wire bonding is used to connect the ICs to the metal paths on the quartz. Although not monolithically integrated, this device incorporates all high frequency components on the quartz substrate so that the packaged part operates in the desired DC in/DC out mode. A photograph of the multi-chip SAW array configuration is shown in Figure 7. The hybrid device requires 90 mA at 2.5 V to operate the GaAs ASICs, which can readily be provided by batteries. The SAW oscillator operates at 510 MHz and the phase comparators have a sensitivity of 1 V per 180 degrees of phase.

These devices have been tested as chemical sensors. The response of the SAW array to dimethyl methyl phosphonate (DMMP) is shown in Figure 15. The varied response of the 3 different coatings indicates their relative sensitivity to DMMP and demonstrates how the array can be used to discriminate among a number of analytes and interferants.

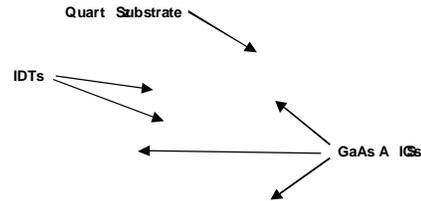


Figure 7. Hybrid version of SAW microsensor array. The ST-quartz die size is 6.9 mm by 8.6 mm. Each of the GaAs ICs is approximately 1 mm x 2 mm. The device operates in a DC in/DC out mode.

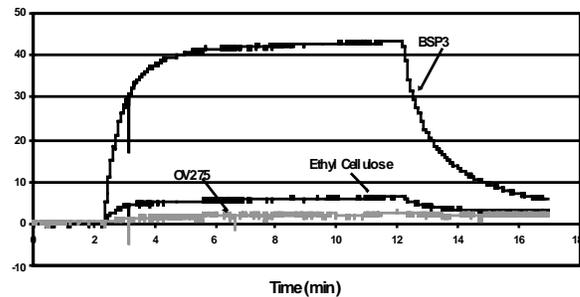
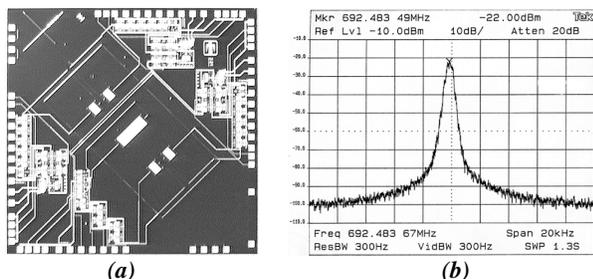


Figure 8. Hybrid SAW array response to 15 parts per million of DMMP. The three microsensor coatings were BSP3 hydrogen-bond acid, ethyl cellulose, and OV-275 (a cyano-modified polysiloxane).

## MONOLITHIC SAW SENSOR ARRAY

We have completed fabrication of the first fully monolithic version of the SAW sensor array described above. This device is based on a GaAs SAW array of the same configuration shown in Figures 4 and 5 and uses the same GaAs microelectronic circuitry as the die shown in Figure 7, but puts all these components onto a single GaAs substrate. Figure 9 (a) shows one of the four-element arrays with the four delay lines arranged diagonally across the center of the die and the amplifier and phase comparator circuitry placed in the corners. The die measures 4.6 mm by 4.6 mm. The microelectronics on the monolithic devices are fabricated at a commercial GaAs IC foundry. The partially processed wafers are transferred to our laboratory for IDT fabrication. Prior to IDT fabrication, a plasma etch is used to remove several microns of dielectric material to expose the GaAs surface. The IDTs are then patterned on the GaAs surface using a metal lift-off process. Figure 9 (b) shows the frequency spectrum of the delay line oscillator portion of the device, which operates at approximately 692.5 MHz and draws 28.5 mA at 3 V<sub>dc</sub>. Oscillator function demonstrates that the post-processing of the IDTs is compatible with the microelectronics fabrication process. The temperature dependence of the phase comparator output has been tested and this is insensitive to temperature, as expected. These devices are now being packaged for further electronic and chemical testing.



**Figure 9. Monolithic GaAs SAW sensor array. (a) Photograph of die showing IDTs in the center and microelectronics in the corners. Die size is 4.6 mm x 4.6 mm. (b) Frequency spectrum of integrated oscillator, demonstrating successful delay line integration.**

## SUMMARY

We have described the development of microfabricated SAW chemical sensor arrays, culminating in a fully monolithic device that integrates all high frequency components onto a single GaAs substrate. These arrays operate in a DC in/DC out mode that simplifies assembly and improves performance. Hybrid arrays show good sensitivity to chemical analytes. Monolithic arrays have shown electronic functionality and are undergoing chemical tests.

## ACKNOWLEDGEMENTS

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# Integrated chemiresistor array for small sensor platforms

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## ABSTRACT

Chemiresistors are fabricated from materials that change their electrical resistance when exposed to certain chemical species. Composites of soluble polymers with metallic particles have shown remarkable sensitivity to many volatile organic chemicals, depending on the ability of the analyte molecules to swell the polymer matrix. These sensors can be made extremely small (< 100 square microns), operate at ambient temperatures, and require almost no power to read-out. However, the chemiresistor itself is only a part of a more complex sensor system that delivers chemical information to a user who can act on the information. We present the design, fabrication and performance of a chemiresistor array chip with four different chemiresistor materials, heaters and a temperature sensor. We also show the design and fabrication of an integrated chemical sensor array, where the electronics for measuring each chemiresistors' resistance are on the same chip with the chemiresistor films. The circuit was designed to perform several functions to make the sensor data more useful. The integrated chemiresistor array's small size and low power demand makes it ideal for deployment on a Sandia-developed microrobot platform.

**Keywords:** Chemiresistor, Sensor Array, Pattern Recognition, Polymer Composite, ASIC, Solvent, VOC, Robot

## 1. INTRODUCTION

Sensors for organic solvent vapors are required for the detection of leaks, toxic chemicals, explosives, and solvent spills. As part of a system, these sensors need to be highly sensitive to small concentrations of vapors in ambient air, while consuming minimal power for use in portable devices. Such a sensor system must be able to quickly and reproducibly distinguish solvents from the ambient relative humidity, and classify the responses as a particular solvent, relative humidity, a mixture, or unknown. The development of a single sensor to distinguish different solvents is difficult; however, sensor arrays with several sensitive devices can be used to sense a wide variety of solvents. Sophisticated pattern-recognition algorithms can aid in the analysis of signals from several sensors in an array and can be used to determine the class of analyte measured.<sup>1-3</sup> A significant amount of research has been performed to develop sensor arrays comprised of several sensitive elements.<sup>4</sup>

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In this paper we discuss chemiresistor arrays fabricated from inks that are solutions of high molecular weight polymers mixed with carbon particles. The preparation of the Sandia inks and the performance of many individual chemiresistors have been presented in several publications.<sup>5-7</sup> Other groups have reported data on similar chemiresistors.<sup>2</sup> If a polymer/conductive particle composite increases its volume by thermal expansion or by swelling when absorbing a chemical, the electrical resistance increases due to the breaking of some of the conductive pathways through the film. The expansion can produce large increases in resistance if the polymer volume is changed close to the percolation threshold.<sup>8-10</sup> This threshold concentration has been found to be between 20 and 40% by volume of the conductive particles. The response of these composite films to different solvents depends on the particular solvent-polymer interaction, while the conductive particles only report the degree of swelling.<sup>5-7</sup> Such materials have been modeled as a network of resistors and diodes, where resistors represent the conductive network of carbon particles and diodes represent the polymer-filled dielectric gaps between the particles.<sup>11</sup>

The degree of swelling of a particular polymer is related to its solubility parameter and the solubility parameter of the solvent. The solubility parameter can be used to describe the free energy of mixing for solvents and polymers. Two solvents that have identical solubility parameter values will form ideal solutions and will have almost zero heat (enthalpy) of mixing. Such ideal solutions of two liquids follow Raoult's law: the vapor pressure of each of the solvents is proportional to the mole fraction of the solvent in the liquid phase. The same rules apply for solvent-polymer mixtures where the amount of solvent-induced polymer swelling depends on the partitioning of the solvent vapor into the polymer film. The lowest detectable concentration of a particular Volatile Organic Chemical (VOC) depends largely on its vapor pressure at ambient temperatures. Very low vapor pressure VOC's can usually be detected at the ppm level if the best polymer for the chemiresistor is chosen.<sup>5-7</sup>

Use of the solubility parameter and the idea of partitioning of the solvent between two phases have already been studied for determining the relative responses of gas sensor arrays.<sup>2,5-7,12</sup> Since it is unlikely that a specific polymer will be sensitive to only one solvent (every polymer absorbs a number of solvents having similar solubility parameters), an array of sensors is an effective means to discriminate against interfering vapors. A common and obvious source of interference is relative humidity in the ambient environment. Water vapor has been found to change the relative sensitivity of certain polymers to solvent vapors and the patterns of responses obtained from arrays containing those polymers.<sup>7,13</sup> To build a sensor array that is capable of identifying the maximum number of analytes, the array should contain several different sensors that are as chemically varied as possible, with at least one sensor having significant sensitivity to relative humidity.

## **2. EXPERIMENTAL DETAILS**

### **2.1. Chemiresistor Array**

A compact array of four different chemiresistors was fabricated on a silicon chip along with two heaters and a temperature sensor. A photograph of one of the arrays is shown in Figure 1. The electrode patterns, temperature sensor, and heaters were made of platinum and titanium created

using standard photolithographic techniques on a silicon wafer with a 200 nm thick insulating silicon nitride layer. The platinum (1000 Å) on titanium (200 Å) features were deposited using evaporation. The low resistance heater strips are at either end of the sensor chip and the temperature sensor is a higher resistance meander line in the center (about 900 ohms). The temperature sensor has a TCR (temperature coefficient of resistance) value of  $0.002^{\circ}\text{C}^{-1}$ . The electrode patterns for the chemiresistors provide for a four-terminal measurement of the resistance with two different spacings for the inner (voltage sensing) electrodes: 50 microns and 100 microns. On each side of the chip there is a set of each of those electrodes. When the mask was designed it was not known if the spacing would have any significant impact on the chemiresistor performance. It turns out that no spacing effects have been discovered for these wide spacings, but earlier electrode arrays with spacings of less than 10 microns had problems with shorting by agglomerated carbon “clumps”. Over 130 sensor arrays can be fabricated on a typical 3-inch diameter wafer. Each different sensor type can be formed on many arrays sequentially, in a batch process mode.

The four different sensors in this particular array were formed from inks as described in references 5, 6, and 7, using the following polymers: poly(n-vinyl pyrrolidone) (PNVP), poly(vinyl alcohol) (PVA), poly(ethylene-vinyl acetate) (PEVA), and poly(isobutylene) (PIB). The sensor electrodes were coated with the chemiresistive inks using an Asymtek Century Series C-702 Automated Dispensing Unit. The 740V Low Viscosity attachment was used with a 27 Gauge, 1/2” needle. The inks were applied to the sensor at a rate of 1.5 inches per second, resulting in a line approximately 500 microns wide by 2300 microns long. The samples were dried at room temperature under ambient conditions. The final dimensions (thickness, width, and length) of the deposited film are highly dependent on the deposition rate and the viscosity of each ink.

This chip has been mounted in a standard 24-pin dual-inline-package (DIP) with the outer dimensions of about 3 cm by 0.7 cm as seen in Figure 1. It can then be inserted in a remote header with ribbon cable to a printed circuit board where the individual resistances can be measured along with the chip temperature. The chip temperature can be controlled above ambient by using a feedback circuit to apply current to the heaters, or for lower power operation at ambient temperature, the chemiresistors can be temperature compensated from their measured TCR values.

## **2.2. Response of the Chemiresistor Array to Volatile Organic Chemicals**

The array was wire bonded into a 24-pin DIP, which could be inserted in a specially designed test fixture. The fixture was attached to a vapor delivery system that had the capability of mixing several gases as well as two solvent vapor streams, using nitrogen as the carrier gas through gas washing bottles (“bubblers”). The bubblers have a wide, porous ceramic frit at the base. Carrier gas is introduced into the solvent through a side arm and up through the frit. The solvent-saturated gas mixture exits the bubbler at the top and is then mixed with pure nitrogen to adjust the solvent concentration as desired. Mass flowmeters were used to control the composition of the gas streams, and a constant total flow rate of  $1000\text{ cm}^3/\text{min}$  was used for all experiments. The test fixture was placed in a constant-temperature chamber, that was maintained at  $21.4^{\circ} \pm 0.3^{\circ}\text{ C}$ . A digital multimeter (7.5 digit resolution) was used to measure the composite-film

resistances. The test gases were passed through a coil of tubing inside the constant-temperature chamber and upstream of the test fixture. This ensured that the inlet gas stream was thermally equilibrated with the sensors. Data acquisition was performed using LabVIEW™ software on a personal computer to control the flow controllers and acquire data from the multimeter.

### 3. RESULTS AND DISCUSSION

#### 3.1. Detection of Solvents

Figure 2 shows the response of three of the four chemiresistors on one of these arrays to a series of pulses of VOC vapors. Dry N<sub>2</sub> flows before and after each pulse of VOC. In each case, the concentration, or partial pressure of the vapor is 10% of the saturated vapor pressure at the bubbler temperature, about 21°C. The reason for using this concentration is given in detail in our previous papers<sup>5-7</sup>, but it involves normalizing out the effect of entropy on the solubility of the vapors in these polymers. If there were no chemical interactions of the vapors with the polymers (i.e. zero heat of mixing), all the signals would be the same size from entropy considerations. The relative differences in the responses then gives a better idea of the relative heats of mixing. By comparing the signals from the three sensors for the various VOCs, it is easy to see that the PVA sensor is more sensitive to polar molecules like water and methanol, while the PEVA sensor more sensitive to less polar molecules.

Data from more than one sensor can be analyzed using pattern recognition algorithms. One such method is the Sandia-developed “Visual Empirical Region of Influence” (VERI), which mimics human vision and classification decisions. Figure 3 shows a “Globe” plot of the data in Figure 2 to demonstrate how one VOC can be distinguished from another by the relative responses. These plots are discussed in our previous papers, but basically they depict a 3-dimensional view of a vector formed from the three sensor signals. The vectors are equalized so that each vector has the same length; i.e. each one extends out to the surface of the unit sphere. The position of a particular point or set of points on the surface of the sphere indicates the response of the array to that analyte. For example, the strong response of PEVA to trichloroethylene (TCE) places the response vector close to the lower left corner. As pointed out in previous publications<sup>3,5-7</sup>, the “VERI” pattern recognition algorithm performs a similar operation to the human vision used in viewing Figure 3 and identifies the VOCs by the clustering of the unknown data points with training data from the known VOCs. Examples of this identification technique have shown that arrays of individual sensors can distinguish many types of solvents, for both pure compounds and binary mixtures, over a wide range of concentrations.

#### 3.2. Analog Chemiresistor ASIC

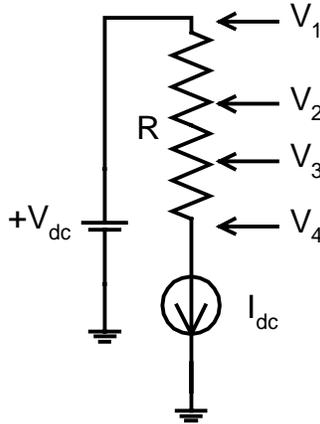
The chemiresistor array shown in Figure 1 is quite small and combines the chemical sensors with an on-chip heater and temperature sensor. But it still requires read-out electronics and controls. A printed circuit board with surface mounted components could provide those functions, but it would require at least a 10-cm by 10-cm board. This size is too large for most micro-robot applications, and this specification led to the design and fabrication of an aluminum-based ASIC (Application Specific Integrated Circuit) to perform resistance measurements and temperature

compensation on a very small footprint. The ASIC was fabricated through MOSIS using AMI's 1.2 $\mu$ m BiCMOS process. This process allows for the use of NPN bipolar transistors along with standard CMOS transistors to make an analog design with a high degree of design flexibility and performance. Circuit simulations were accomplished using Pspice<sup>®</sup> and circuit layout was done using L-Edit<sup>™</sup>. The integrated chemiresistor ASIC also allows multiple sensors to be fabricated on a single substrate. A photo of the four sensor ASIC array is given in Figure 4. In this design each chemiresistor is connected to its own analog electronics. This was done so each chemiresistor could be individually temperature compensated by the on-chip electronics, which use individual calibrations for dc set point and temperature compensation. Having the chemiresistor and electronics co-located with the integrated circuit minimizes undesired temperature responses by using the reduced size to minimize any cross-chip temperature gradients. The bonding (I/O) pads are arranged around the edges to make it easier to wirebond the whole array to a substrate. Future improvements in the ASIC circuit will include the use of digital pots to perform the chemiresistor baseline corrections and temperature compensation. The current ASIC design and footprint allow room for additional circuitry if needed.

A photomicrograph of one chemiresistor ASIC diced out of the wafer is shown in Figure 5. The chemiresistor itself is on the left side covering most of the four parallel electrodes. The outer, current injecting electrodes were made wider to facilitate charge injection, while the inner, voltage pick-off electrodes were made narrower to give an accurate voltage drop measurement. The bonding pads around the edges allow various test voltages to be measured and provide links to the off-chip input voltages, calibration resistors, and the sensor output voltages. The entire ASIC is coated with a thin layer of silicon dioxide glass, except for the bonding pads and regions where the chemiresistor film is deposited on the electrodes.

In addition to the integrated circuit design, which needs to be flexible enough to accommodate a variety of chemiresistor base resistances, TCRs and signal magnitudes, the electrodes for the sensor can not be made from aluminum because of severe contact resistance problems between the polymer films and Al electrodes. Wafer level post-processing of the ASIC chemiresistive sensor to deposit a platinum (1000 Å) on titanium (200 Å) overlayer, by evaporation, on top of the aluminum electrodes was accomplished using a metal lift-off technique. Clariant AZ 9245 resist was used as a masking material, and the sensor area was exposed using a Karl Suss MA6/BA6 contact aligner. Titanium and platinum were sequentially deposited using a Temescal CV-8 metal evaporator.

To help reduce contact resistance effects, a four-point probe measurement is used to measure each chemiresistor film. The circuit for the four-point measurement is depicted in the following diagram:



To measure a segment of the resistor,  $R$ , independent of  $V_{dc}$ , two voltage measurements  $V_2$  and  $V_3$  are made and the incremental resistance,  $R_i$  is calculated by  $R_i = (V_2 - V_3)/I_{dc}$  where  $I_{dc}$  is the known current from a current source. For the chemiresistor ASIC, it was desired to have an analog voltage that effectively measures the chemiresistor and provides a convenient output signal for use with commercial or custom telemetry units.

The measurement described here has the following practical limitations:  $V_{dc}$  must be greater than  $I_{dc} \cdot R$  due to the fact that the practical current source must be biased at least slightly above ground, and to select a current source value the nominal baseline resistance value must be known before hand.

The method chosen for the four-point measurement employs a precision voltage controlled current source with a feedback loop that servo the voltage  $V_{drop} (= V_2 - V_3)$  to a predetermined value, usually 1.0 volts. The voltage applied to the voltage controlled-current-source will provide a large dynamic range signal that indirectly measures an incremental part of the chemiresistor. This measurement is independent of  $V_{dc}$  and allows a temperature compensation scheme in that the value of  $V_{drop}$  can easily be made a linear function of temperature, thus negating the chemiresistor temperature dependence.

The chemiresistor ASIC includes a linear temperature compensation scheme, as seen in Figure 6. This circuit uses a voltage-controlled current source to servo a voltage,  $V_{drop}$ , to a desired value, approximately 1.0 volts. The desired static value of  $V_{out1}$  and the value of the calibration resistor and the temperature compensation circuit determine the actual value of  $V_{drop}$ .  $V_{out1}$  is defined as

$$V_{out1} = 4 V_{drop} R_{cal}/R_{chem}, \quad (1)$$

where  $V_{drop} = V_{constant} + V_{temp}$ .  $V_{drop}$  is nominally adjusted from 1.0 volts. The dc voltage,  $V_{out1}$ , is nominally adjusted to 3.5 volts.  $R_{cal}$  is the calibration resistor and  $R_{chem}$  is the measured incremental value of the chemiresistor.  $R_{cal}$  is used to adjust the  $V_{out1}$  baseline voltage with the chemiresistor exposed to ambient or dry air.  $V_{temp}$  is a temperature dependent variable used to cancel the temperature dependence of  $R_{chem}$ . This variable can be adjusted for both positive and negative temperature coefficients via select resistors. The temperature coefficient of the chemiresistor can be negated by the analog circuit through a range of 0 to  $\pm 4\%/^{\circ}\text{C}$ . The

reference used for this temperature compensation circuit comes from the  $-2\text{mV}/^\circ\text{C}$  temperature response of a bipolar transistor base-emitter voltage ( $V_{be}$ ). Since this compensation is open-loop and linear to temperature the temperature coefficient and linearity of the chemiresistor must be known or the substrate operating temperature range must be limited.

To make the monitoring of small signals easier, a high gain output feature was added to the ASIC circuit. This output,  $V_{out2}$ , is an amplified (10x)  $V_{out1}$ , defined as

$$V_{out2} = 10 (V_{out1} - V_{offset}) + V_{offset}. \quad (2)$$

The circuit baseline is adjusted for  $V_{out1}$  and  $V_{out2}$  to be approximately 3.5 volts, which is accomplished by adjusting the calibration resistor and  $V_{offset}$ , respectively.  $V_{offset}$  has a nominal value of 3.5 volts. These adjustments are performed using resistor elements external to the ASIC. The output  $V_{out1}$  also has the feature of accommodating large dynamic swings in the chemiresistor resistance. As was shown in references 5-7, the chemiresistor resistance change becomes superlinear (almost exponential) at higher concentrations of the VOCs. In fact the resistance will increase several decades as the concentration approaches the saturated vapor pressure of some VOCs. The circuit output compresses these large changes with a loss of resolution, but not the saturation effect that occurs with a linear output circuit. This circuit design accommodates a relatively large dynamic range of  $R_{chem}$  because the circuit response is a function of  $1/R_{chem}$ . The change in resistance over at least two decades can be monitored with this circuit with reasonable resolution.

### 3.3. Integrated Chemical Microsensor Robot

As an example of the utility of integrated microsensors we show a recently developed Sandia microrobot prototype which uses the integrated chemiresistor. The details of the fabrication of this microrobot and its performance will be given in a future publication. Some of its features are given in Figure 7. The wheels have been removed from the small drive motors for clarity. The other two corners have casters on them. The substrate for the electronics board is a lithium battery. The IR communications port provides line-of-sight data transfer and commands along with an IR proximity detector to prevent collisions with other objects. One can imagine other types of mobile micro-platforms that could use the integrated chemiresistor ASIC: flying machines, submarines and inconspicuous sensor emplacements.

## 4. CONCLUSIONS

In this paper we have shown how a simple chemical sensor technology, the chemiresistor, can be implemented in a system with very small size and power consumption. The response of the chemiresistor itself has been measured for a wide variety of VOCs, but in a small system the measurement circuitry must be integrated and perform a number of housekeeping functions to provide useful information to the overall system for decision making. We have presented an integrated prototype sensor and have shown how it can fit into a microrobot platform, whose specifications require low power operation, low weight, small size.

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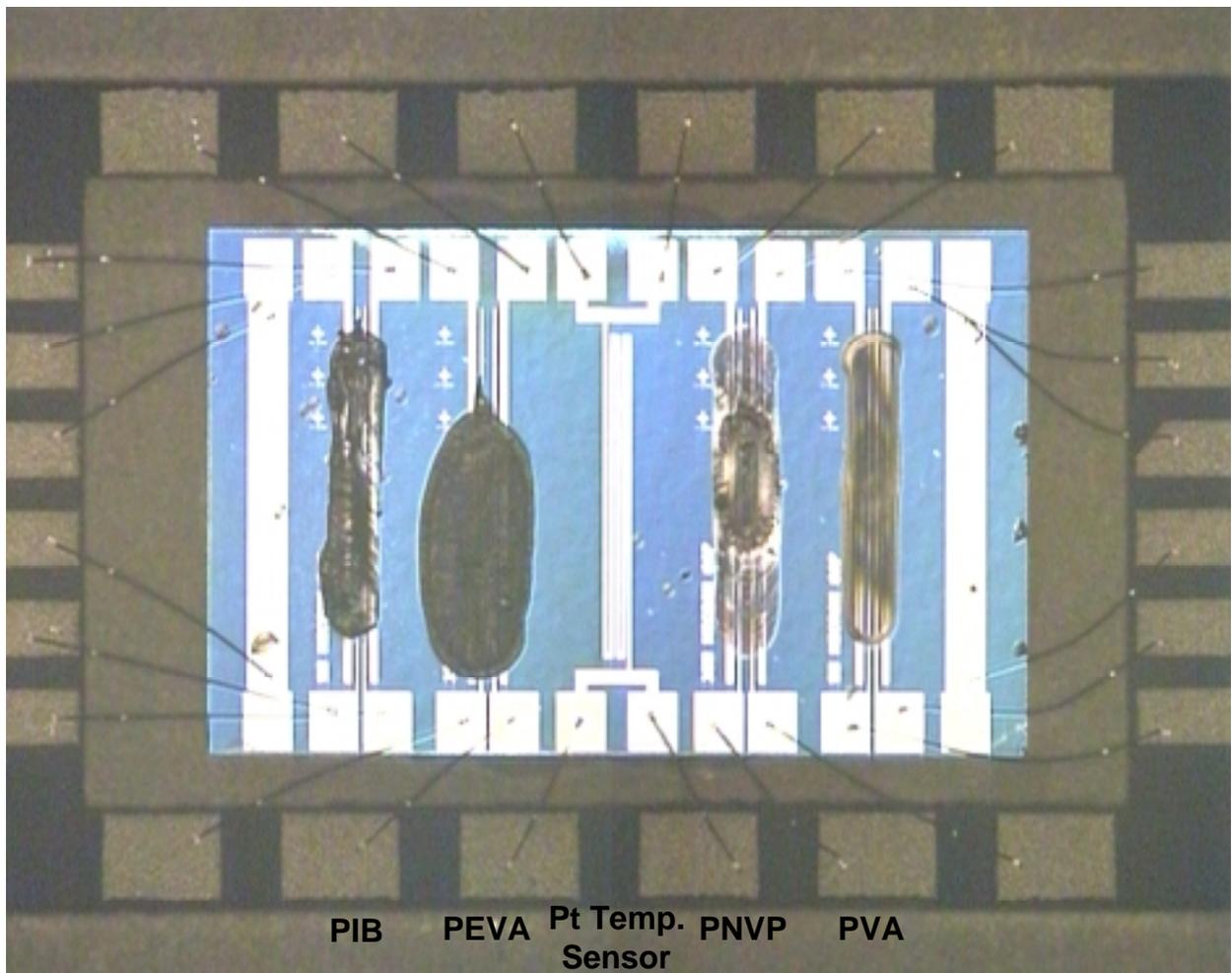


Figure 1. Four different chemiresistor polymers on the array chip, which is 8 mm by 4 mm and mounted in a standard 24 pin DIP. The polymers are defined in the text.

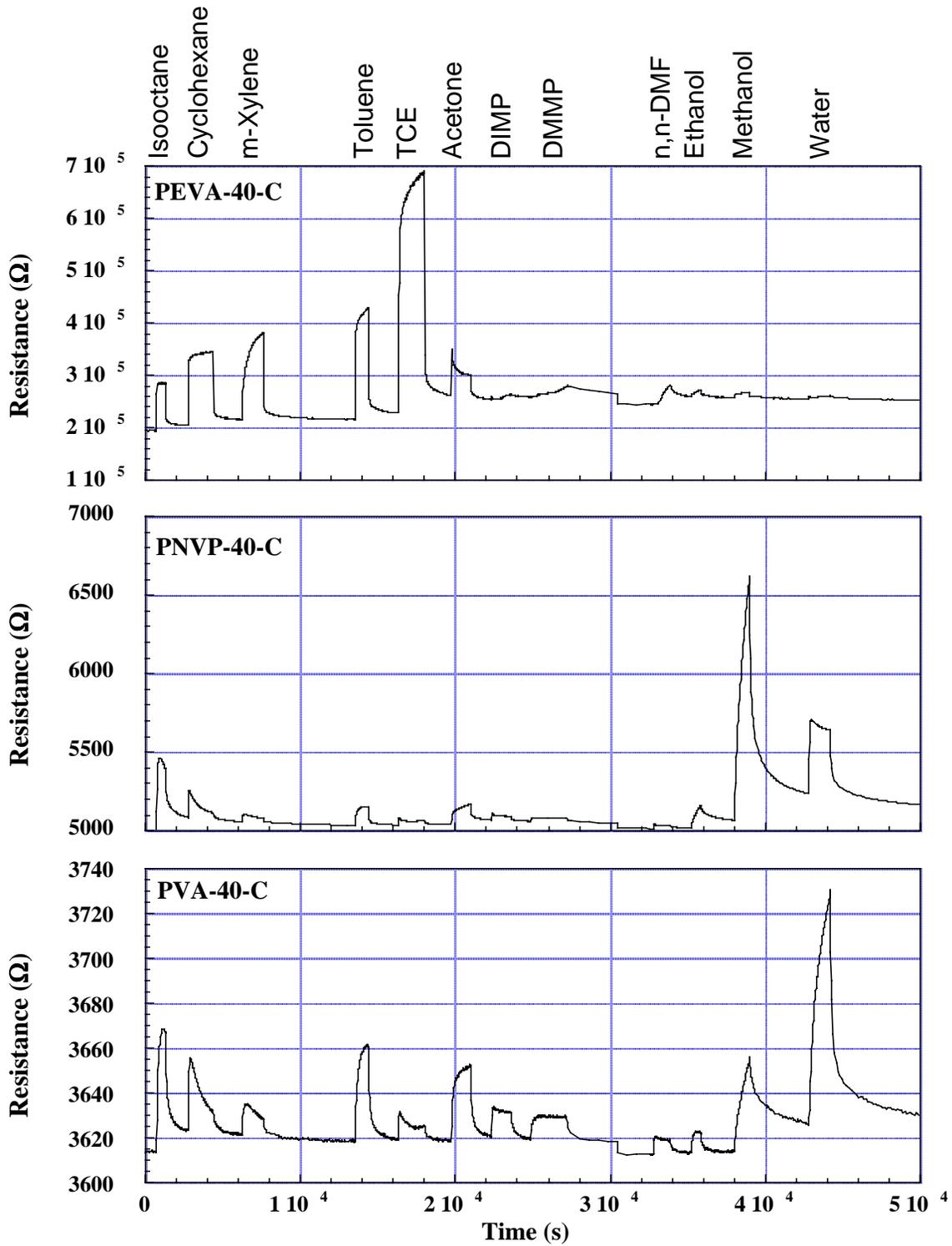


Figure 2. The responses of three of the chemiresistors on the array to a variety of volatile organic chemicals (VOCs). Each pulse of VOC is followed by a dry  $N_2$  purge.

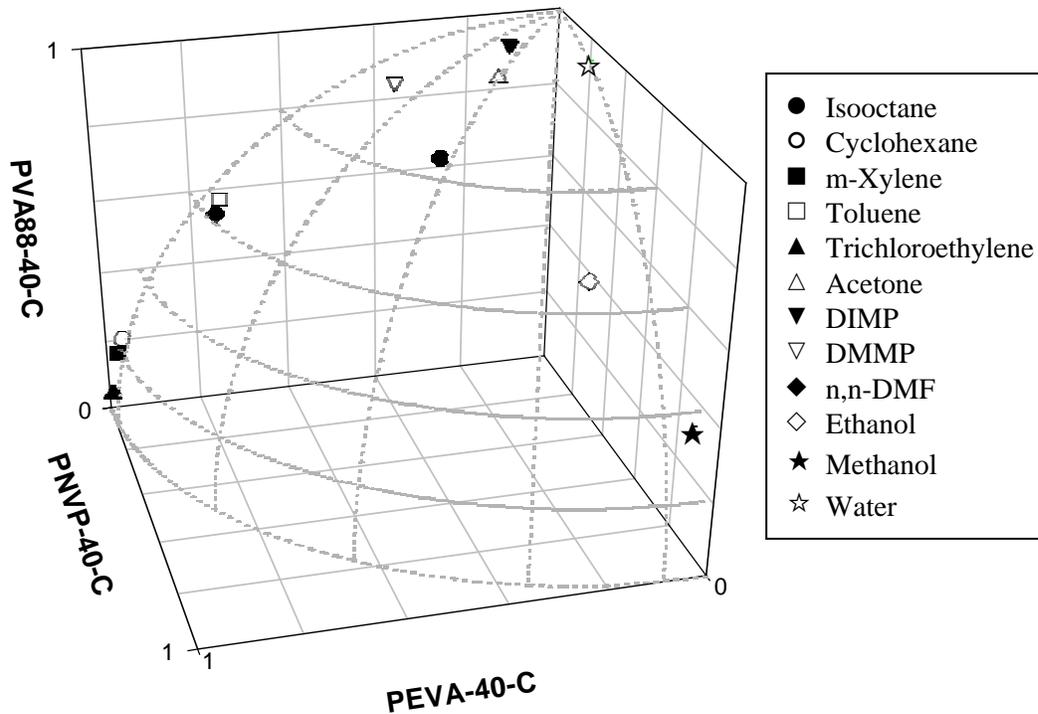


Figure 3. The same data as in Fig. 2 replotted for pattern recognition by transforming the response of each VOC to a 3-D vector equalized to fit on a unit sphere. Most are easily identified in this fashion by their vector position on the sphere

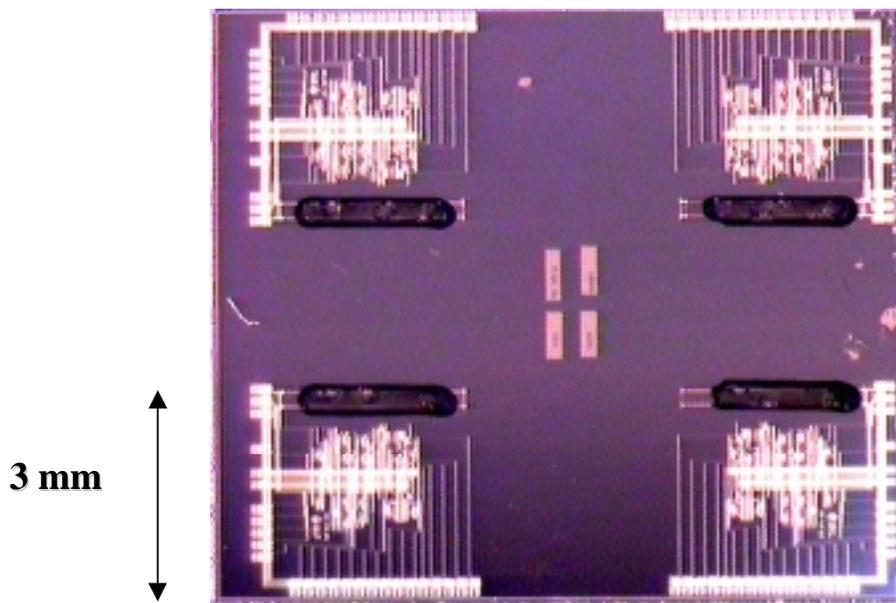


Figure 4. The Sandia Integrated Chemiresistor Array composed of four chemiresistors on their electrodes with the individual ASIC circuits for measuring the chemical responses and correcting for temperature changes.

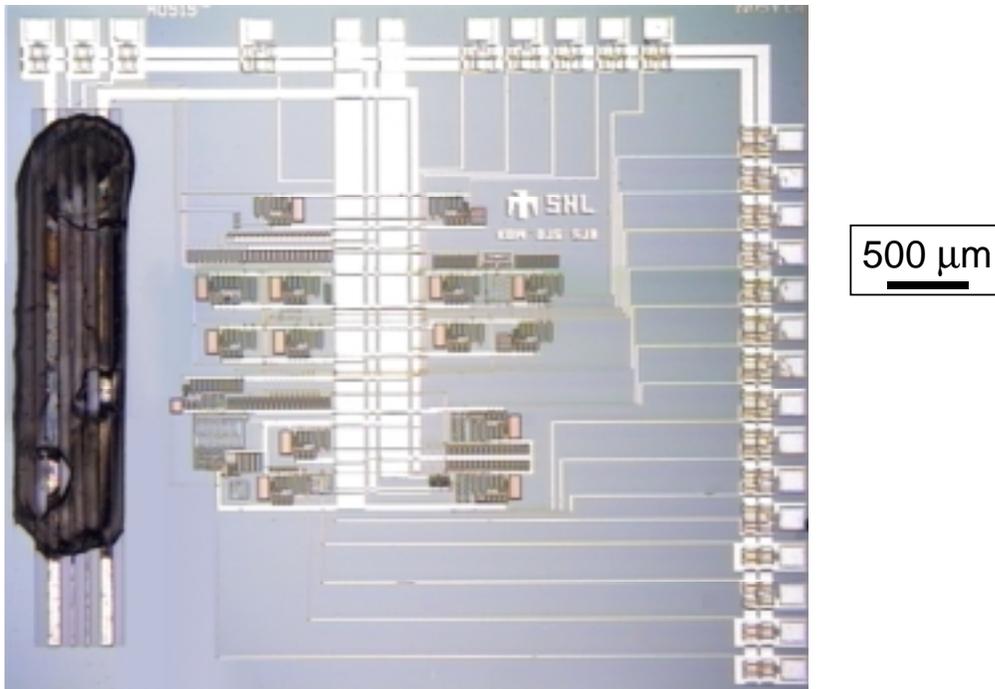


Figure 5. A close-up of one of the ASICs showing the electrode pattern (Pt/Ti over Al by post-processing), the ASIC circuit elements and the bonding pads.

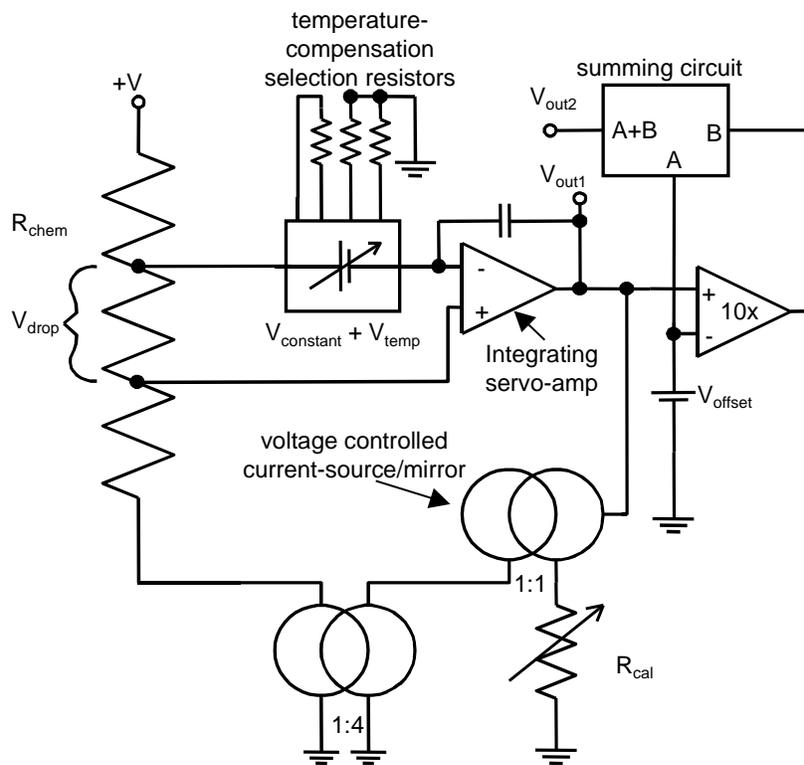


Figure 6. Schematic of ASIC circuit.

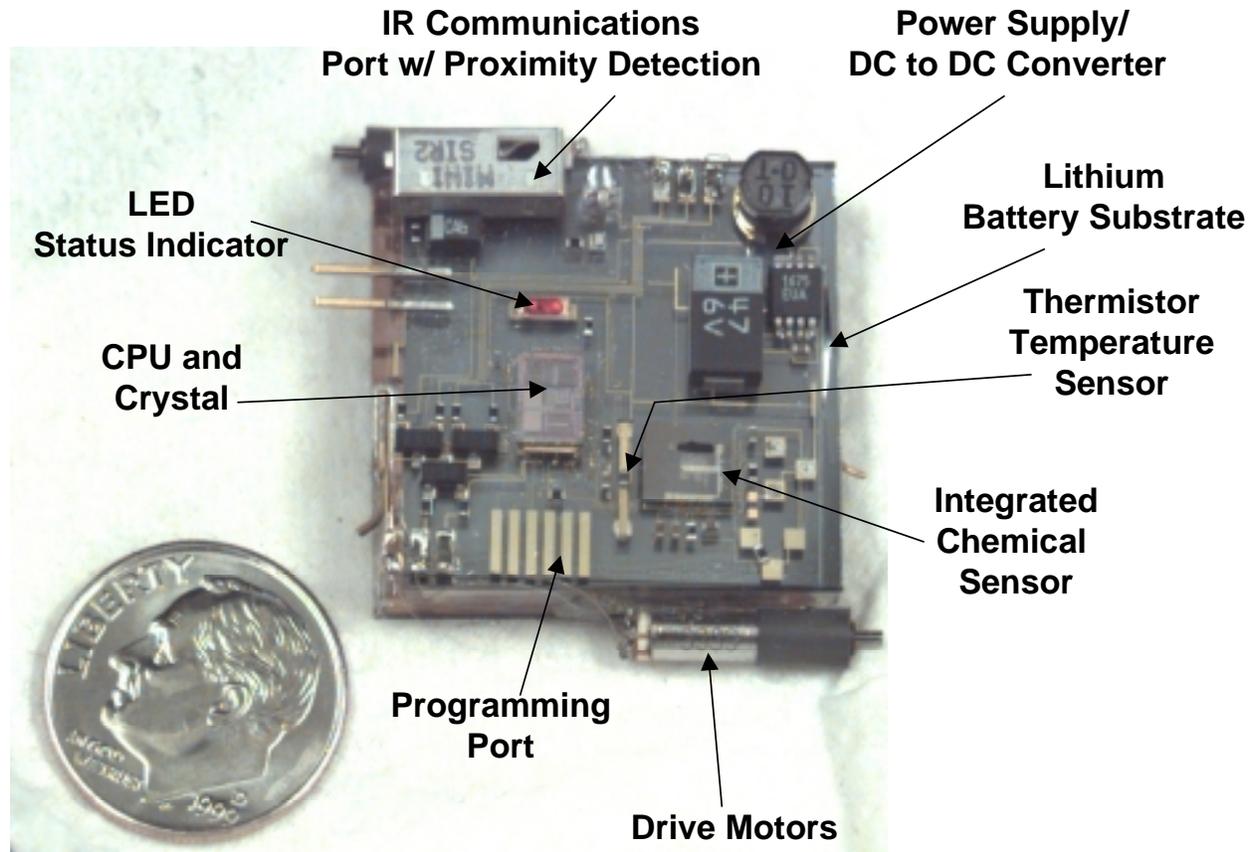


Figure 7. A prototype microrobot with the Integrated Chemiresistor Array wire bonded to the base PC board. The wheels have been removed from the drive motors for clarity.